UCD Viewer

USER MANUAL

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Table of Contents

1. ABOUT THIS MANUAL

Purpose

This guide is the User Manual of UCD-1 MLC, UCD-1 QLV and UCD-2 Vx1, USB-connected video capture units for use in a PC with Windows® 8, Windows® 7 or Windows® XP operating system.

The purpose of this guide is to

- Provide an overview of the product and its features.
- Provide instruction for the user on how to install the software and the drivers.
- Introduce the HW features of the units.
- Provide instructions for the user how use the UCD Viewer software.

Product and Driver Version

This manual explains features found in UCD Software Package **1.6.** Please consult Unigraf for differences or upgrades of previous versions.

Please consult the Release Notes document in the installation package for details of the SW versions and changes to previous releases.

Notes

On certain sections of the manual, when important information or notification is given, text is formatted as follows. Please read these notes carefully.

Note	This text is an important note

2. HARDWARE

First, shared hardware properties for each UCD device are described and later the device specific features are presented.

Figure 1 UCD-1 device back panel

Figure 2 UCD-2 device back panel

Connectors

USB

USB 2.0 Hi-Speed standard type-B connector. There is no power draw from this connector.

Power

Switchcraft S761K external power connector.

Pin	Description
1. Tip	+5VDC
2. Sleeve	Ground

Sync Out, Sync In

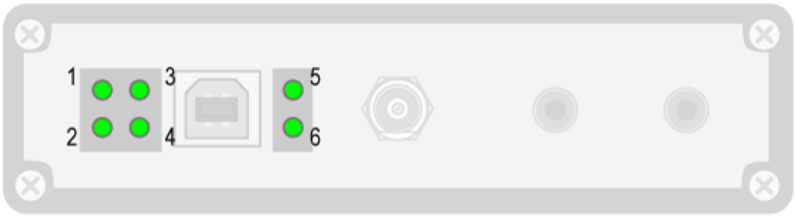
Synchronization output and synchronization input for master slave configuration of capturing multiple parallel channels.

Pin	Description
1. Tip	Signal 1
2. Ring	Signal 2
3. Sleeve	Ground

Status LEDs

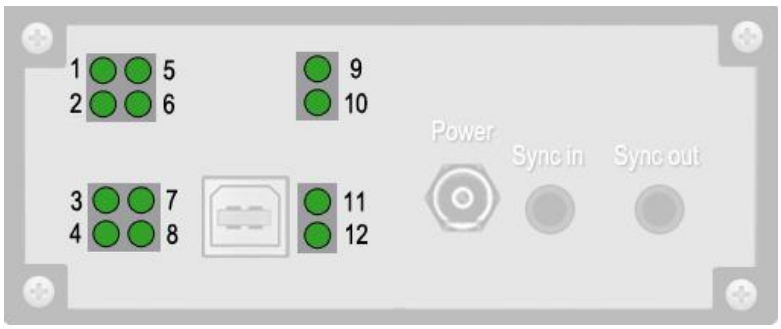
LED operations of UCD devices are firmware dependent and subject to change excluding *power good* which is always available. Functions for each LED are described in the figure below.

UCD-1 Devices



LED	Function	Description
1	ON / Flashing	Frame ready CH1 A / B, turns OFF when frame read
2	Flashing	FW running
3	N/A	Undefined
4	ON	Power Good
5	ON / Flashing	Frame ready CH2 A / B, turns OFF when frame read
6	Flashing	FW running

UCD-2 Vx1



LED	Description
1, 3, 9, 11	On = V-by-One symbol lock
2, 4, 10, 12	Flashing = FW running
6, 8	On = Power good
7	For chained devices: On = Master, Off = Slave
5	Unused

Memory

The table below shows the available frame buffer memory capacity in different data configuration cases. Since captured data is stored as 8-bit bytes regardless of color depth setting (6 / 8 bits per color) each color component will use 8 bits of memory.

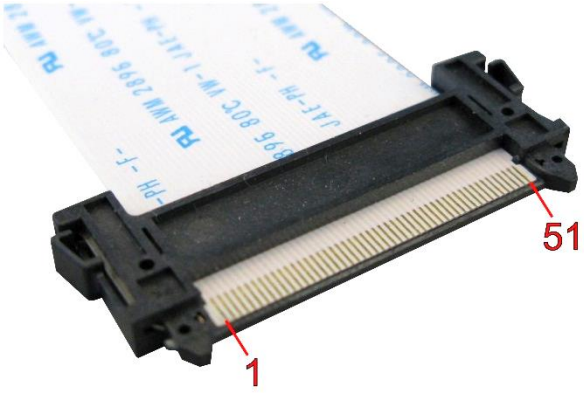
Case	Frame Buffer Capacity
1 Channel, 3 pairs	50331648 Samples (equals to 8 Full HD (1920 x 1080) frames)
1 Channel, 6 pairs	100663296 Samples
2 Channels, 6 pairs	201326592 Samples
4 Channels, 6 pairs	402653184 Samples

UCD-1 MLC

Display Signal Input Connectors

JAE FI-RE51 series high-speed connector (device has FI-RE51S-HF-R1500). Cable contacts are facing down when connecting connector to device.

Note:	These connectors are fragile and they are locking. Please make sure that you release the latches when removing. Please use care when you plug and unplug them.



Please find pinouts for the mini-LVDS (UCD-1 MLC) and Quad LVDS (UCD-1 QLV) cases in the table presented on the next page.

UCD-1 mini-LVDS pinout

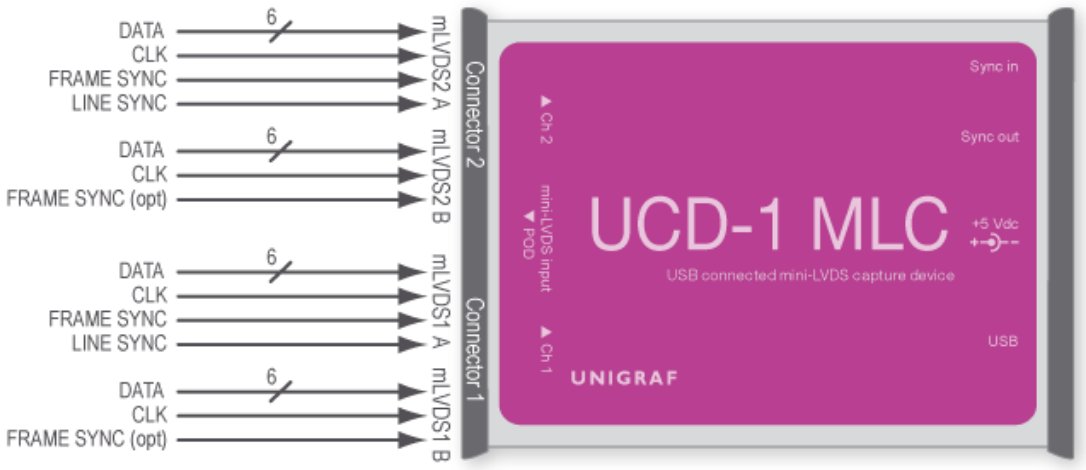
The table below shows the pin-out of one connector. Please refer to chapter Connecting Source Devices later in this document on allocating data to the two connectors.

Channel A is for the data of left (primary) and Channel B of right (secondary) pixels. N/C = No Connection

Pin	Signal	Description	Pin	Signal	Description
1	POD_+5PW	N/C / Not in use	25	CHB_N0	Channel B, Lane 0 Negative
2	POD_+5PW	N/C / Not in use	26	CHB_P0	Channel B, Lane 0 Positive
3	POD_+5PW	N/C / Not in use	27	CHB_N1	Channel B, Lane 1 Negative
4	POD_+5PW	N/C / Not in use	28	CHB_P1	Channel B, Lane 1 Positive
5	POD_+5PW	N/C / Not in use	29	CHB_N2	Channel B, Lane 2 Negative
6	GND	Signal Ground	30	CHB_P2	Channel B, Lane 2 Positive
7	GND	Signal Ground	31	GND	Signal Ground
8	GND	Signal Ground	32	CHB_CKN	Channel B, Clock Negative
9	GND	Signal Ground	33	CHB_CKP	Channel B, Clock Positive
10	CHA_N0	Channel A ,Lane 0 Negative	34	GND	Signal Ground
11	CHA_P0	Channel A, Lane 0 Positive	35	CHB_N3	Channel B, Lane 3 Negative
12	CHA_N1	Channel A, Lane 1 Negative	36	CHB_P3	Channel B, Lane 3 Positive
13	CHA_P1	Channel A, Lane 1 Positive	37	CHB_N4	Channel B, Lane 4 Negative
14	CHA_N2	Channel A, Lane 2 Negative	38	CHB_P4	Channel B, Lane 4 Positive
15	CHA_ P2	Channel A, Lane 2 Positive	39	GND	Signal Ground
16	GND	Signal Ground	40	TP	N/C
17	CHA_CKN	Channel A, Clock Negative	41	CHB_N5	Channel B, Lane 5 Negative
18	CHA_CKP	Channel A, Clock Positive	42	CHB_P5	Channel B, Lane 5 Positive
19	GND	Signal Ground	43	GND	Signal Ground
20	CHA_N3	Channel A, Lane 3 Negative	44	CHA_N5	Channel A, Lane 5 Negative
21	CHA_P3	Channel A, Lane 3 Positive	45	CHA_P5	Channel A, Lane 5 Positive
22	CHA_N4	Channel A, Lane 4 Negative	46	GND	Signal Ground
23	CHA_P4	Channel A, Lane 4 Positive	47	CHA_FS	Channel A, mini-LVDS Frame Start, +3.3V logic level
24	GND	Signal Ground	48	GND	Signal Ground
			49	CHA_LS	Channel A, mini-LVDS Line Start, +3.3V logic level
			50	GND	Signal Ground
			51	CHB_LS	Channel B, mini-LVDS Line Start, +3.3V logic level

POD

This connector is unused with current firmware. Please leave unconnected.



Connecting mini-LVDS Source Devices

UCD-1 MLC has four mini-LVDS data channels with each having six data pairs and one clock pair. Each channel has a line sync signal input. Frame sync signal is shared between two channels on the same connector.

All UCD-1 channels are expected to have the same data and clock setups. Please find below example configurations of connecting the data lines.

Example Source	mLVDS1 A	mLVDS1 B	mLVDS2 A	mLVDS2 B
1 channel: 6 data pairs + 1 clock pair	6 x data (0-5) 1 x clock	N/A	N/A	N/A
2 channels: 8 data pairs + 2 clock pairs	4 x data (0-3) 1 x clock	4 x data (0-3) 1 x clock	N/A	N/A
4 channels: 24 data pairs + 4 clock pairs	6 x data (0-5) 1 x clock	6 x data (0-5) 1 x clock	6 x data (0-5) 1 x clock	6 x data (0-5) 1 x clock
4 channels: 4 data pairs + 4 clock pairs	1 x data (0) 1 x clock	1 x data (0) 1 x clock	1 x data (0) 1 x clock	1 x data (0) 1 x clock

UCD-1 QLV

UCD-1 Quad LVDS pinout

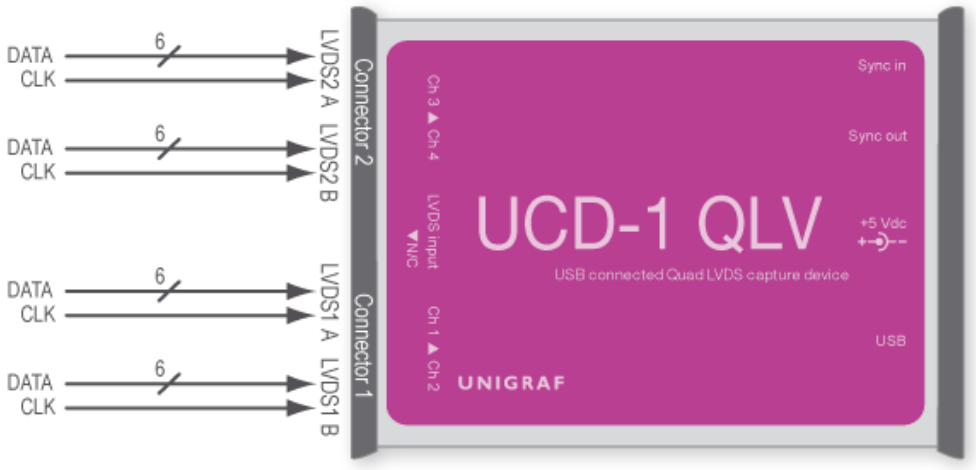
The table below shows the pin-out of one connector. Please refer to chapter Connecting Source Devices later in this document on allocating data to the two connectors.

Pin	Signal	Description	Pin	Signal	Description
1	POD_+5PW	N/C / Not in use	25	CHB_N0	Channel B (even), Lane 0 Negative
2	POD_+5PW	N/C / Not in use	26	CHB_P0	Channel B, Lane 0 Positive
3	POD_+5PW	N/C / Not in use	27	CHB_N1	Channel B, Lane 1 Negative
4	POD_+5PW	N/C / Not in use	28	CHB_P1	Channel B, Lane 1 Positive
5	POD_+5PW	N/C / Not in use	29	CHB_N2	Channel B, Lane 2 Negative
6	GND	Signal Ground	30	CHB_P2	Channel B, Lane 2 Positive
7	GND	Signal Ground	31	GND	Signal Ground
8	GND	Signal Ground	32	CHB_CKN	Channel B, Clock Negative
9	GND	Signal Ground	33	CHB_CKP	Channel B, Clock Positive
10	CHA_N0	Channel A (odd), Lane 0 Negative	34	GND	Signal Ground
11	CHA_P0	Channel A, Lane 0 Positive	35	CHB_N3	Channel B, Lane 3 Negative
12	CHA_N1	Channel A, Lane 1 Negative	36	CHB_P3	Channel B, Lane 3 Positive
13	CHA_P1	Channel A, Lane 1 Positive	37	CHB_N4	Channel B, Lane 4 Negative
14	CHA_N2	Channel A, Lane 2 Negative	38	CHB_P4	Channel B, Lane 4 Positive
15	CHA_ P2	Channel A, Lane 2 Positive	39	GND	Signal Ground
16	GND	Signal Ground	40	TP	No connection
17	CHA_CKN	Channel A, Clock Negative	41	CHB_N5	Channel B, Lane 5 Negative
18	CHA_CKP	Channel A, Clock Positive	42	CHB_P5	Channel B, Lane 5 Positive
19	GND	Signal Ground	43	GND	Signal Ground
20	CHA_N3	Channel A, Lane 3 Negative	44	CHA_N5	Channel A, Lane 5 Negative
21	CHA_P3	Channel A, Lane 3 Positive	45	CHA_P5	Channel A, Lane 5 Positive
22	CHA_N4	Channel A, Lane 4 Negative	46	GND	Signal Ground
23	CHA_P4	Channel A, Lane 4 Positive	47	N/C	N/C / Not in use
24	GND	Signal Ground	48	GND	Signal Ground
			49	N/C	N/C / Not in use
			50	GND	Signal Ground
			51	N/C	N/C / Not in use

Channel A is for the data of ODD (1st) and Channel B of EVEN (2nd) pixels. N/C = No Connection

POD

This connector is unused with current firmware. Please leave unconnected.



Connecting LVDS Source Devices

UCD-1 QLC has four mini-LVDS data channels with each having six data pairs and one clock pair. LVDS sync is embedded in the data lanes.

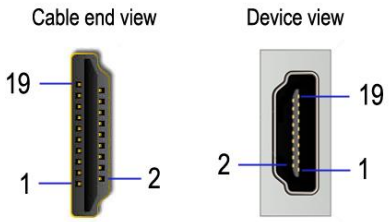
All UCD-1 channels are expected to have the same data and clock setups. Please find below example configurations of connecting the data lines.

Example Source	LVDS1 A	LVDS1 B	LVDS2 A	LVDS2 B
1 channel: 6 data pairs + 1 clock pair	6 x data (0-5) 1 x clock	N/A	N/A	N/A
2 channels: 12 data pairs + 2 clock pairs	(Channel 1) 6 x data (0-5) 1 x clock	(Channel 2) 6 x data (0-5) 1 x clock	N/A	N/A
4 channels: 24 data pairs + 4 clock pairs	(Channel 1) 6 x data (0-5) 1 x clock	(Channel 2) 6 x data (0-5) 1 x clock	(Channel 3) 6 x data (0-5) 1 x clock	6 x data (0-5) 1 x clock

UCD-2 VX1

V-by-One Inputs

V-by-One inputs use 19 pin HDMI connectors (device has Molex 47266-0001). Connectors are described in detail in the figure below.



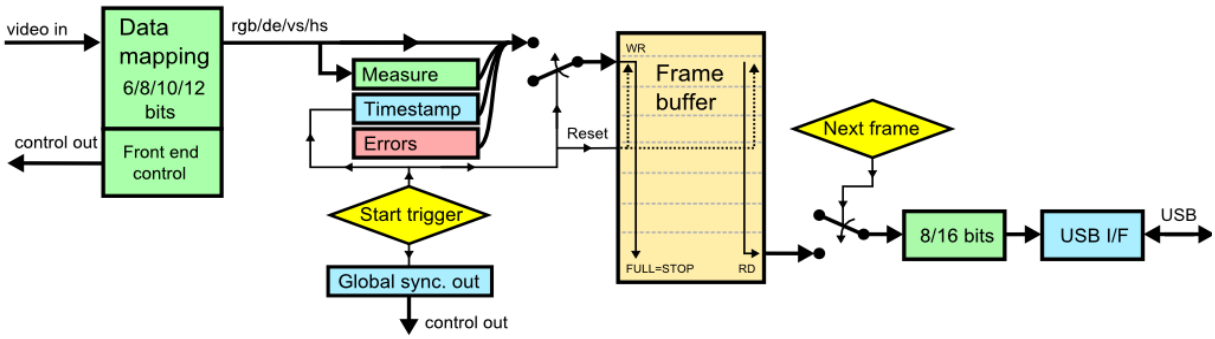
The following table describes function of each pin for each connector.

Pin number	Connector 5	Connector 6
1	Lane 8 +	Lane 4 +
2	Lane 8 shield / Ground	Lane 4 shield / Ground
3	Lane 8 -	Lane 4 -
4	Lane 7 +	Lane 3 +
5	Lane 7 shield / Ground	Lane 3 shield / Ground
6	Lane 7 -	Lane 3 -
7	Lane 6 +	Lane 2 +
8	Lane 6 shield / Ground	Lane 2 shield / Ground
9	Lane 6 -	Lane 2 -
10	Lane 5 +	Lane 1 +
11	Lane 5 shield / Ground	Lane 1 shield / Ground
12	Lane 5 -	Lane 1 -
13	Unconnected	Unconnected
14	Unconnected	Unconnected
15	Unconnected	LOCKn
16	Unconnected	HTPDn
17	Ground	Ground
18	Unconnected	Unconnected
19	Unconnected	Unconnected

Capture Process

UCD hardware blocks are described in the figure below. Simplified version of the capture process is described as follows:

1. Set V-by-One color depth (6/8/10/12 bits /V-by-One byte mode)
2. Choose the desired number of V-by-One lanes to be captured.
3. Set color depth (8/16 bits) that is transferred over USB to PC. This setting affects data amount i.e. preview frame rate. It does not need to be the same as V-by-One color depth chosen in step 1.
4. Trigger capture start.
5. Video frames are saved to memory until memory is full.
6. Frames are readable one by one from the memory until memory is empty.
7. To continue, go back to step 4.

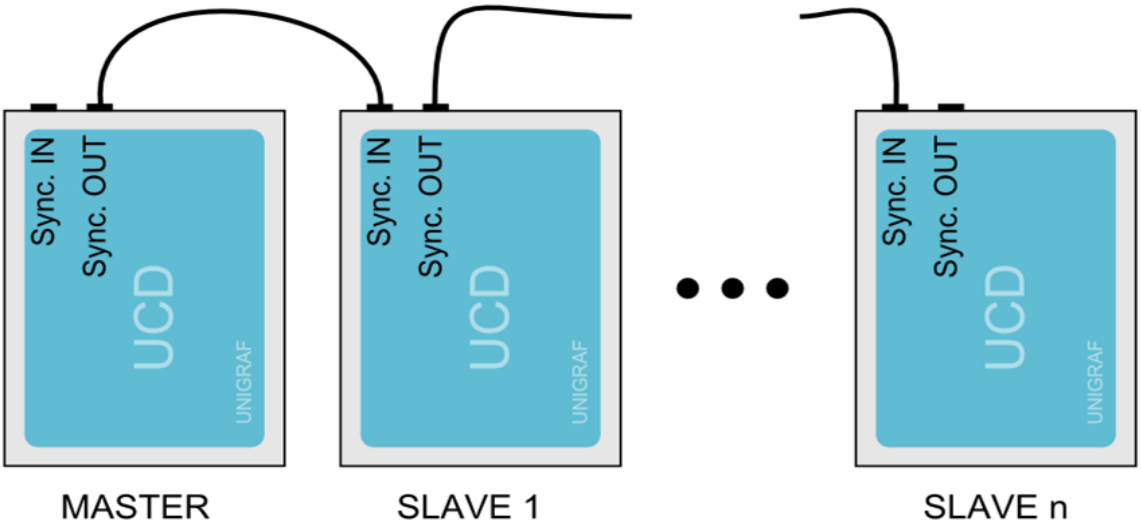


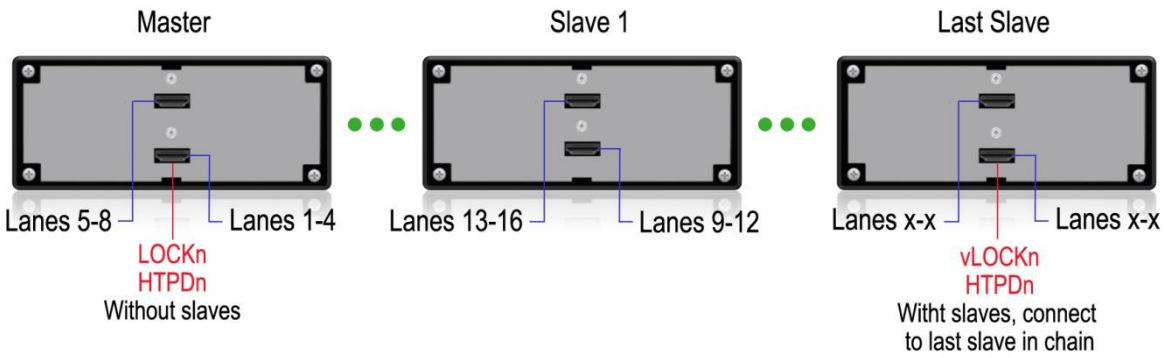
Device chaining

Two or more UCD-2s can be chained together for capturing more than 8 lanes. The connection is done with a synchronizing cable as shown in the figure below. Figure in the following page shows the intended V-by-One connections in a chained configuration.

When chaining devices, please pay attention to the following:

- Device chain must not form a ring.
- Both ends of the cables should always be connected to a device.
- All devices must be connected to the same computer via USB cables.
- LOCKn and HTPDn must be connected to correct devices for reliable operation.
- Please not that connecting the lanes incorrectly does not prevent capturing but will only affect visible video.





External Trigger

An external trigger can be used to start video capture precisely at the right time. Connect the external trigger to the Sync IN input (pin 2, See Fig. 9). The trigger should provide a 3.3V logical levels. Video capture can be started by either rising or falling edge.

The trigger input is internally pulled up (10kΩ resistor) to 3.3V. It enables triggering the video capture manually with a push button that simply grounds the input (short pins 2 and 3 and trigger to falling edge).

External trigger mode needs to be enabled by setting the option value UUCD_OPTION_EXT_TRIGGER to either EXT_TRIGGER_FALLING or EXT_TRIGGER_RISING. Setting the option to EXT_TRIGGER_NONE disables external trigger mode.

Exactly like in free-run mode, the application should invoke UUCD_StartCapture() and then it can read frames by calling UUCD_GetFrame() until all the buffered frames are transferred to a PC. In external trigger mode, the first UUCD_GetFrame() call may take long time as it will be waiting for an external trigger to start video capture. Consider setting long enough timeout by calling SetOption() with UUCD_OPTION_FRAMEINFO_TIMEOUT parameter.

If UCD-2 devices are chained, the master device propagates the trigger to all slave devices. All chained devices start video capture synchronously.

3. UCD VIEWER

Unigraf UCD Viewer software is the configuration and capture GUI for UCD-1 and UCD-2 devices. UCD Viewer can be used with mini-LVDS (UCD-1 MLC), Quad LVDS (UCD-1 QLV) and V-by-One (UCD-2 Vx1) capture. First, shared properties for each UCD device are described and later the device specific features are presented.

System requirements

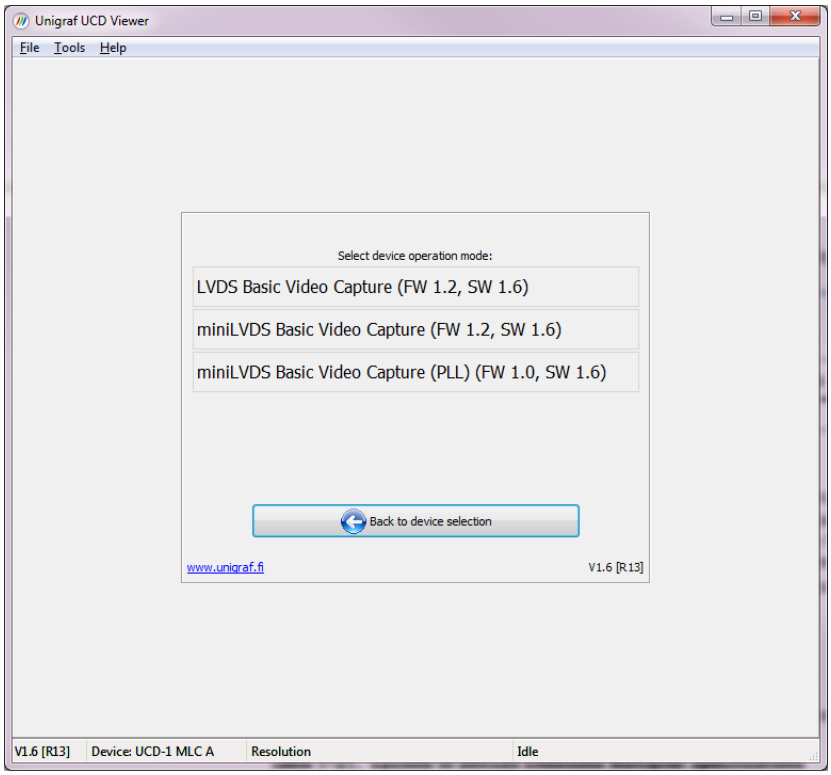
The UCD Viewer application can be used in 32-bit and 64-bit editions of Windows XP, Windows Vista, Windows 7 and Windows 8.

Installation

UCD Viewer can be installed by running **UCD Setup.exe.** The installer will allow you to select the components used and configure the install locations.

Device and Mode Selection

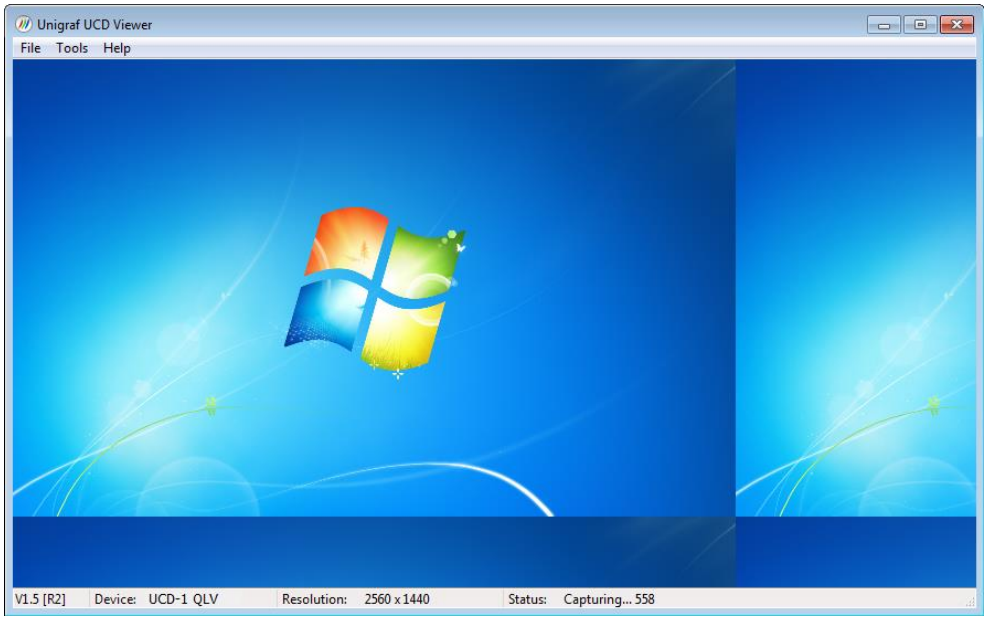
When *UCD Viewer* is launched, you can first select the connected UCD device.



In the following dialog you can select the signal mode that you want to use. Please select **LVDS Basic Video capture** for Quad LVDS signal and **miniLVDS Basic Video Capture** or **miniLVDS Basic Video Capture (PLL)** for mini-LVDS. Two options are provided for mini-LVDS. The first will sample in data directly with incoming mini-LVDS clock and the second will feed mini-LVDS clock into a PLL circuit before sampling in data. The controls of the configuration dialog will be different in the two cases.

Preview Window

When you click **Start capture** a window will open and show a preview of your captured content.



You can align the size of the preview window to the content by right clicking on top of the window and selecting one of the **fixed zoom factors** 25% [Alt+1], 50% [Alt+2] or 100% [Alt+3].

You can display the captured content in a borderless window by selecting **Borderless Mode**. You can also maximize the window on your desktop by selecting **Maximize**.

Controls

You can end the current session by selecting **File > Stop Capture.**

You can select another capture device by selecting **File > Close Device**. From the dialog click the new capture device that you need to use.

Saving

- By selecting **File > Save snapshot (Ctrl+S)** you can capture and save individual frames. By selecting **File > Save video sequence** you can save a sequence of captured frames.

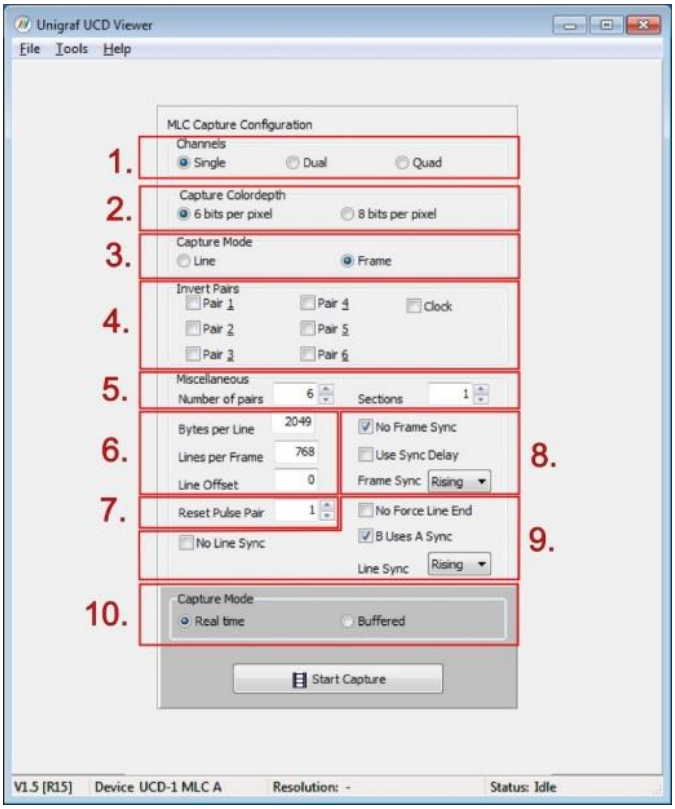
Capture Format

- You can select the capture image format from **Tools > Options**. The available formats are PPM (up to 16 bpc), BMP and JPG (8 bpc).

  In the same dialog you can also select the folder where the image files are stored.

UCD-1 MLC

mini-LVDS Mode



MLC Capture Configuration

Section 1. Channels:	
Single	CH1 A is used.
Dual	CH1 A, CH1 B is used.
Quad	CH1 A, CH1 B, CH2 A, CH2 B is used.
Section 2: Capture Colordepth:	
6 bits per pixel	Data is serialized in 6 bits samples.
8 bits per pixel	Data is serialized in 8 bits samples.
Section 3: Capture Mode	
Line	Device outputs data one line per read.
Frame	Device outputs frames.
Section 4: Invert Pairs	
Tick any box to swap differential pair positive and negative for that pair. The same setting will be applied to all channels.	

Miscellaneous:

Section 5:	
Bytes per line	Number of captured samples in a mini-LVDS line including all data pairs (must be divisible with “Number of pairs” in current Viewer version)
Lines per frame	Number of mini-LVDS lines in a frame (NOTE: some devices output R/G/B in separate lines i.e. this value is set to 3x resolution)
Line Offset	Offset from *frame sync* signal to video line start, signed value. Set this value (trial and error) last after you can capture stable video.
Section 6:	
6 bits per pixel	Data is serialized in 6 bits samples.
8 bits per pixel	Data is serialized in 8 bits samples.
Section 7:	
Reset Pulse Pair	Differential pair that has a stable mini-LVDS line reset pulse (line start marker). Same setting is applied to all channels. Normally set to 1.
Section 8:	
No Frame Sync	When set device tries to find a vertical blanking area between lines to split data into frames. Normally frame sync should be used
Use Sync Delay	When set device adds internal delay to frame sync signal. Set this if frame sync is close to a line start and video output jumps up and down one line.
Frame Sync	Set to rising or falling edge sync
Section 9:	
No Line Sync	When set device will only try to find line reset pulses (line starts). In this mode device may sync to frame video data depending on video content (e.g. vertical white bar in middle of frame). Normally when not set, line sync makes device to search reset pulse during horizontal blanking area.
No Force Line End	When set device will not cut line length when line sync signal is found. Set this if line sync is found during active video. Normally, line sync should mark the end of line data and be set after active video has already stopped.
B Uses A Sync	Set this if there is only one line sync signal per channel connector.
Line Sync	Set to rising or falling edge sync.
Section 10: Capture Mode	
Real Time	Frame buffer is flushed after one frame is read out from buffer.
Buffered	Frame buffer is flushed after all frames have been read out from buffer.

Settings Example

Please find below an example on how to configure a mini-LVDS source. The source has the following characteristics:

- Resolution: 1920x1080
- Pairs: 6 data + 2 clocks
- Serialization / color depth: 6 bits
- Synchronization: Has frame sync and only one line sync

Configuration Item	Setting
Number of Pairs	CH1A has 3 pairs and CH1B has 3 pairs (because of two clocks cannot use same channel)
Channels	Dual, see Number of Pairs
Capture Color Depth	User should know this or try either value
Capture Mode	Frame, Line mode only needed if device cannot sync to frames and requires manual work to construct a frame.
Invert pairs	Depends on signal routing. If e.g. captured frame has a black bar on the left (width of sync pulse) sync pair is probably inverted.
Bytes per Line	CH1A has 960 pixels and CH1B has 960 pixels (expecting one line gives RGB data / whole pixels) 2* 960 pixels * 3 colors = 5760 samples (CHA and CHB will always capture same number of samples)
Lines per Frame	1080, because lines have RGB data (any value should work here i.e. can be 100 or 4000). Use with “Line Offset” to get the best view.
Line Offset	Set to a value where you see the first line in top of the frame. Use trial and error and positive and negative values.
B Uses A Sync	Must be set (only 1 sync available, duplicated inside device)
No Frame Sync	Has a frame sync, not selected
No Line Sync	Has a line sync, not selected
No Force Line End	User should select this at first try and later unselect it if capturing works without it.
Reset Pulse Pair	User must find with trial and error
Sections	1, this option is not fully supported with current SW. User software must adjust sections correctly.
Capture Mode	Both options should work

UCD-1 QLV

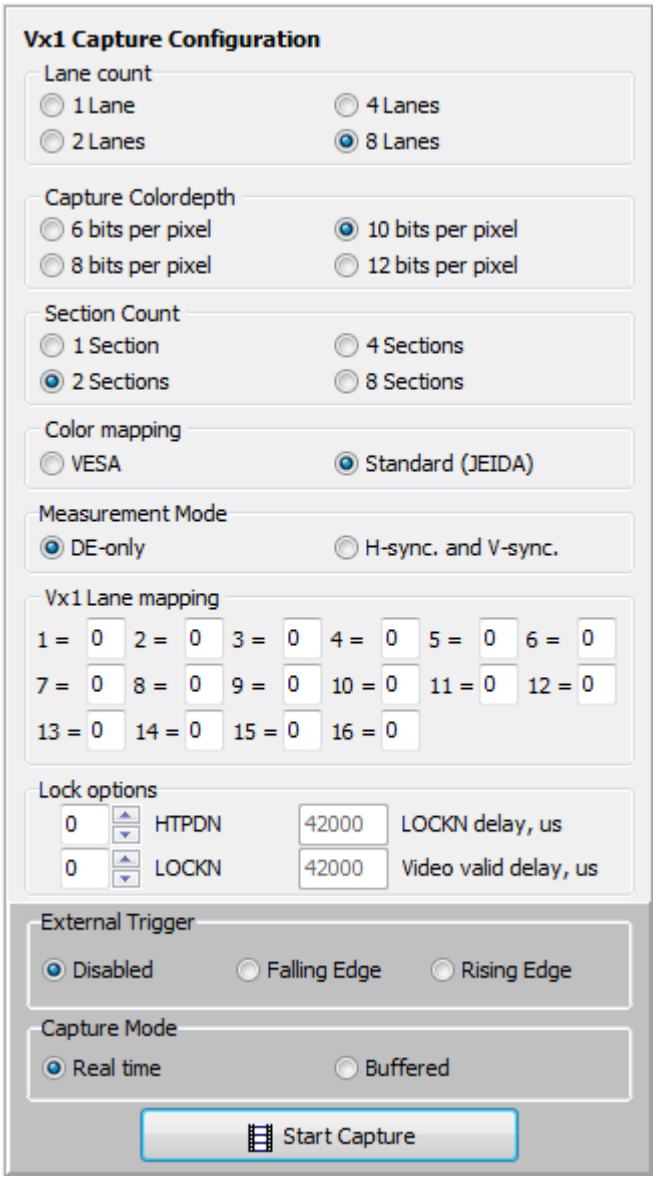
Quad LVDS Mode

Capture Mode:	
Single	CH1 A is used.
Dual	CH1 A, CH1 B is used.
Quad	CH1 A, CH1 B, CH2 A, CH2 B is used.
Capture Colordepth:	
6 bits per pixel	Color data is in 6 bits samples (3 data pairs per channel).
8 bits per pixel	Color data is in 8 bits samples (4 data pairs per channel).
10 bits per pixel	Color data is in 10 bits samples (5 data pairs per channel).
12 bits per pixel	Color data is in 12 bits samples (6 data pairs per channel).
Color mapping	
VESA	VESA LVDS data mapping is used.
JEIDA	JEIDA LVDS data mapping is used.
Section 10: Capture Mode	
Real Time	Frame buffer is flushed after one frame is read out from buffer.
Buffered	Frame buffer is flushed after all frames have been read out from buffer.

UCD-2 Vx1

Vx1 Basic Video Capture Configuration

In the following window you can select the preferred Vx1 Capture Configuration settings. Vx1 Capture Configuration settings are described in the figure below.



<table>
<tr><th>Setting</th><th colspan="4">Descripiton</th></tr>
<tr><td>Lane count</td><td colspan="4">Number of lanes to capture. For cascaded devices, it shows the total number of lanes for all devices.</td></tr>
<tr><td>Capture color depth</td><td colspan="4">Selects input color-depth and capture color-depth. The preview display is always 24 bit true-color, while saved file will have the requested color-depth.</td></tr>
<tr><td>Section count</td><td colspan="4">Number of sections the frame is divided into.</td></tr>
<tr><td>Color mapping</td><td colspan="4">Selects color-mapping mode. (Vx1 should always use JEIDA).</td></tr>
<tr><td>Measurement Mode</td><td colspan="4">DE-only or Hsync-VSync based measurement</td></tr>
<tr><td>Vx1 Lane mapping</td><td colspan="4">All zero means that default mapping is used (= No change of lane order). This feature can be used to correct a situation where the Vx1 lanes are mixed up for some reason. For example, if lanes 1 and 2 are reversed on the physical connector, enter 2 to the first edit box, and 1 to the second.
Note: This function is only software data rearrange. It means that e.g. 4 lane capturing needs to have all 4 lanes connected to lanes 1,2,3 and 4 for device to achieve lock to input signal.</td></tr>
<tr><td>External trigger</td><td colspan="4">Controls using external trigger mode, see 2.7</td></tr>
<tr><td rowspan="3">Capture mode

Lock Options</td><td colspan="4">In real time mode, the internal UCD-2 device buffer memory is not used, it only stores one frame. the screen is updated with minimal delay but some frames might be lost due to limited USB2 band width. In the buffered mode, a sequence of frames is stored in the internal buffer memory and then transferred to the PC. There are no frame gaps in this sequence. There may be gaps between sequences.

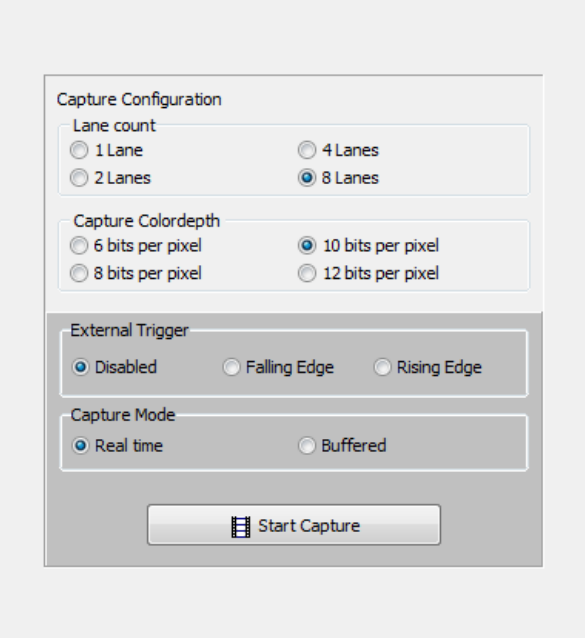
Adjust the needed delay period based on product specifications. For the configuration rules, follow the table below.</td></tr>
<tr><td>HTPDN:
0 = Normal operation (Default)
1 = HTPDn signal is forced low
2 = HTPDn signal is forced high</td><td>LOCKN
0 = Normal operation (Default)
1 = LOCKn signal is forced low
2 = LOCKn signal is forced high
3= LOCKn signal is forced low, and stays low, after "LOCKN delay" time has elapsed. Timer starts after HTPDn goes low internally in normal operation. Setting of "HTPDN" value does not affect this timer.</td><td>LOCKN delay, us:
Timer value in micro seconds to "LOCKN" option 3. Default is 42000 us.</td><td>Video valid delay, us:
Timer value in micro seconds after which valid video is received from source after LOCKn signal goes low. Setting "LOCKN" option 1 or 2 does not prevent timer operation. Default is 42000 us.</td></tr>
</table>

After selecting the settings you can start the acquisition by pressing '**Start Capture**' button. You can return to the configuration window by selecting "**Stop Capture**" from the

"**File**" option in the main menu. To return to the device selection window, select "**Close device**" from the "**File**" option in the main menu.

When capture is in progress, single frame capture and frame-sequence capture features are available through the " **File**" option in the main menu. Captured frames are stored in files according to the settings in "**Tools**" → "**Options**" dialog described in chapter 3.5.

Internal pattern generator



Settings are similar to those described in Vx1 Basic Video Capture Configuration.

APPENDIX A. PRODUCT SPECIFICATION

UCD-1 MLC

Image Data Input	4 parallel mini-LVDS channels with 6 data lanes. Divided in 2 groups. 1 frame start input per group, 1 lane start input per channel.
Input Connector	3 x FI-RE51S-HF-R1500 (JAE Electronics) (2 x for data lanes 1 x for control)
Link Speed	270 MHz maximum
Input Configuration	6 or 8 bits / link Sync In / Out Synchronizing input and output for Master / Slave configuration
Capture Speed	Approximately 4 FHD frames / second
Computer interface	USB 2.0
Software	Windows 8, 7 and XP, Linux UCD Viewer application for Windows SDK SW API with Example and preview
Power supply	AC/DC Power supply (100 to 240 Vac 50/60 Hz input, +5 Vdc output)
Mechanical Size	170 × 128 × 33 mm
Weight	0.4 kg w/o power supply

UCD-1 QLV

Image Data Input	4 parallel LVDS channels with 6 data lanes. Clock input for Each channel
Input Connector	3 x FI-RE51S-HF-R1500 (JAE Electronics) (2 x for data lanes 1 x for control)
Pixel Rate	100 MHz / channel maximum
Input Configuration	Input Configuration 6, 8, 10 or 12 bits / color Sync In / Out Synchronizing input and output for Master / Slave configuration
Pixel Mapping	VESA and JEIDA
Capture Speed	Approximately 4 FHD frames / second
Computer interface	USB 2.0
Software	Windows 8, 7 and XP, Linux UCD Viewer application for Windows SDK SW API with Example and preview
Power supply	AC/DC Power supply (100 to 240 Vac 50/60 Hz input, +5 Vdc output)
Mechanical Size	170 × 128 × 33 mm
Weight	0.4 kg w/o power supply

UCD-2 Vx1

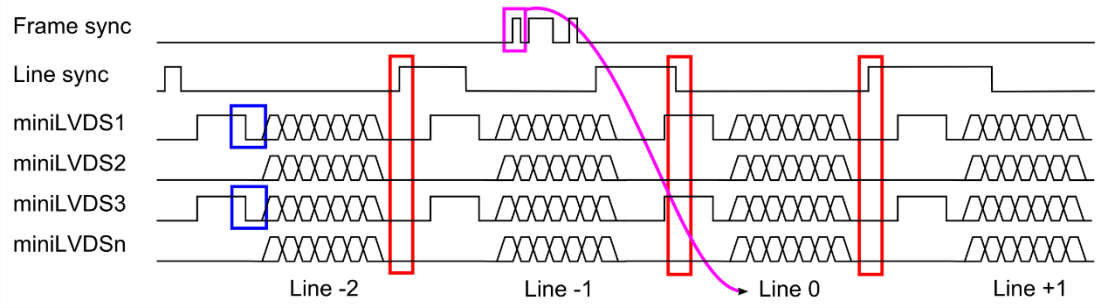
Power Requirement	
Supply voltage	+5VDC ±15%
Supply current	< 3A
Performance	
25MB/s	USB transfer, typical (root dependent)
8	Lanes
3.75Gb/s	V-by-One data rate / Lane
20MHz – 75MHz	Pixel clock / Lane @ 5 byte mode
20MHz – 85MHz	Pixel clock / Lane @ 4 byte mode
20MHz – 100MHz	Pixel clock / Lane @ 3 byte mode
Operating Environment	
Operation temperature	+10°C – +40°C
Storage temperature	+0°C – +60°C

Frame Buffering		
256 Frames	16.77 MPixels Memory / Lane	
Buffering Examples		
Video Mode	Lanes	Buffered Frames
1920×1080 @ 60Hz	2	16
1920×1080 @ 60Hz	4	32
1920×1080 @ 240Hz	8	64
4096×2160 @ 60Hz	8	15
4096×2160 @ 120Hz	16 (chained)	30

All specifications are subject to change without notice.

APPENDIX B: MLVDS SYNCHRONIZATION

The image below describes the synchronization signal cases that UCD-1 MLC (mini-LVDS) recognizes. UCD-1 MLC samples the frame synchronization and line synchronization signals using mini-LVDS data clock. The mini-LVDS data clock (double data rate) is not shown in the image.



Reset Pulse

The blue boxes in the image show the end of the reset pulse the start of data. In this example the reset pulse can be taken either from miniLVDS1 or miniLVDS3 pair.

Line Sync

The red boxes in the image show a correct line synchronization signal edge in three different cases. Line sync can be the TP1 signal in Mini-LVDS specification.

- The box on the left shows a valid rising edge. Also, falling edge would work with the left case.
- The box in the middle box shows a valid falling edge. The rising edge of the same pulse is during a data period and cannot be used.
- The box on the right shows a case where the falling edge of the pulse is during a data period. In this case the rising edge will be chosen.

Frame Sync

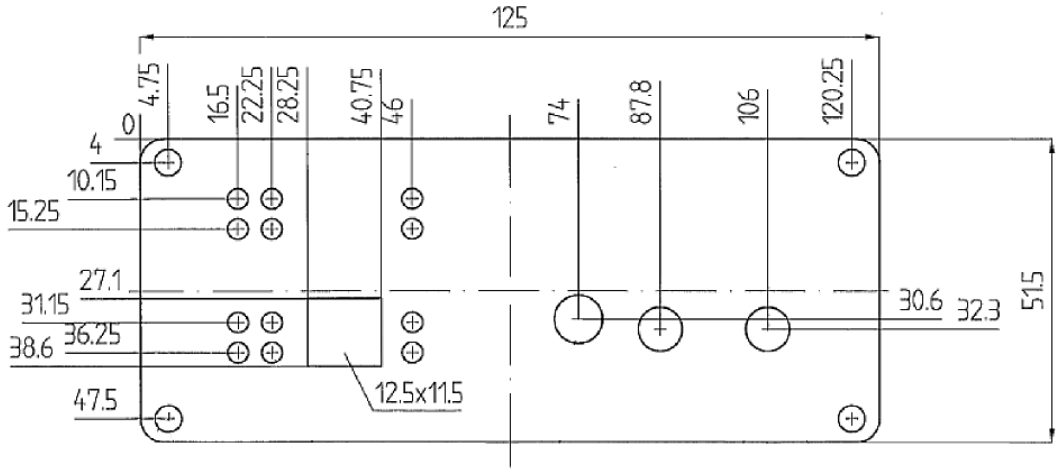
The magenta box shows a valid frame synchronization marker. UCD-1 accepts the first edge and ignores any consecutive edges for the duration of approximately one frame period. This means the frame sync can be a pulse train.

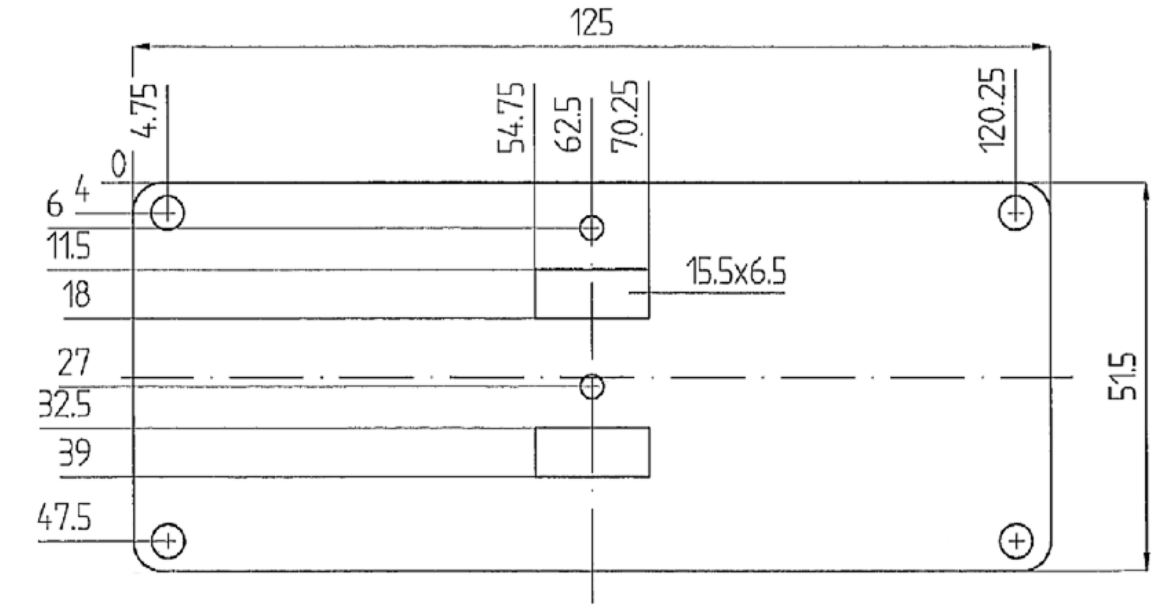
Frame sync must come during every (captured) frame and during the same frame line number. The data line following the frame sync will assigned as line number zero. In the GUI the user will indicate the positive or negative offset of line number zero to the first line of the frame.

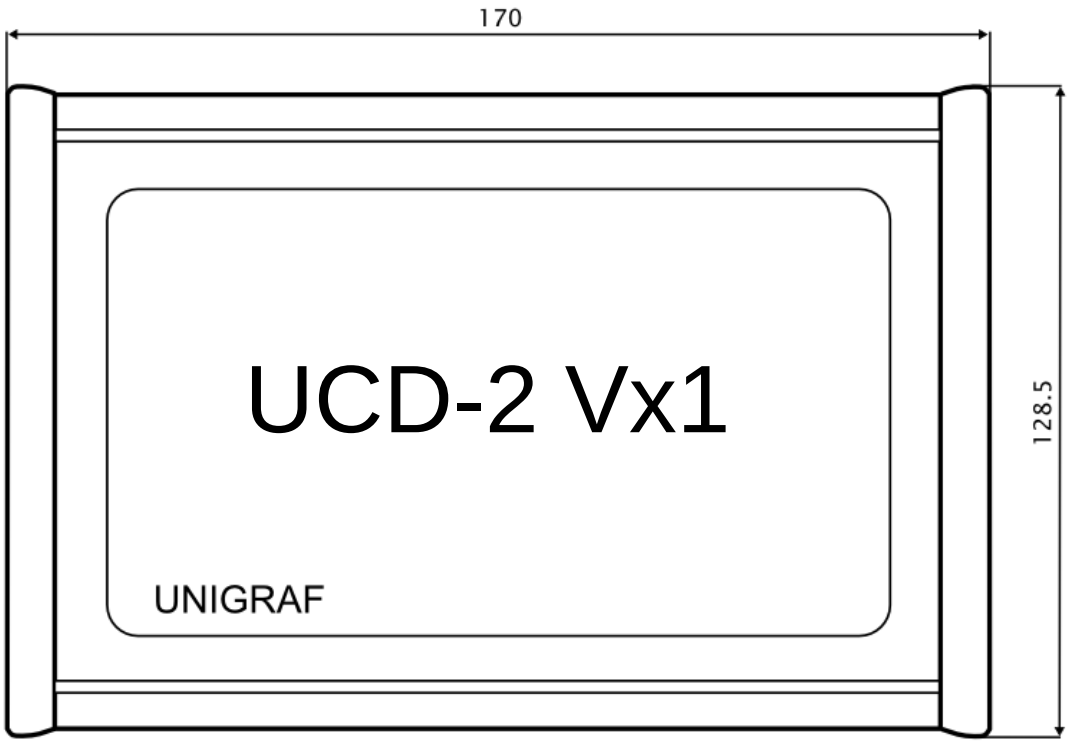
APPENDIX C: PHYSICAL DIMENSIONS

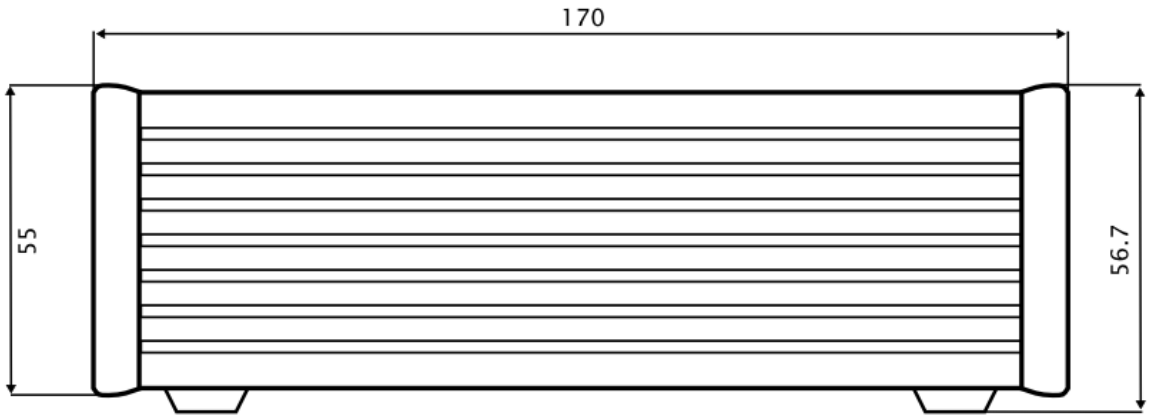
All UCD devices have lightweight aluminum casing with plastic rims. All lengths are given in mm.

UCD-2 Vx1






170
UCD-2 Vx1
UNIGRAF
128.5


170
55
56.7