Introduction to LTTPR

Link-Training Tunable PHY Repeaters
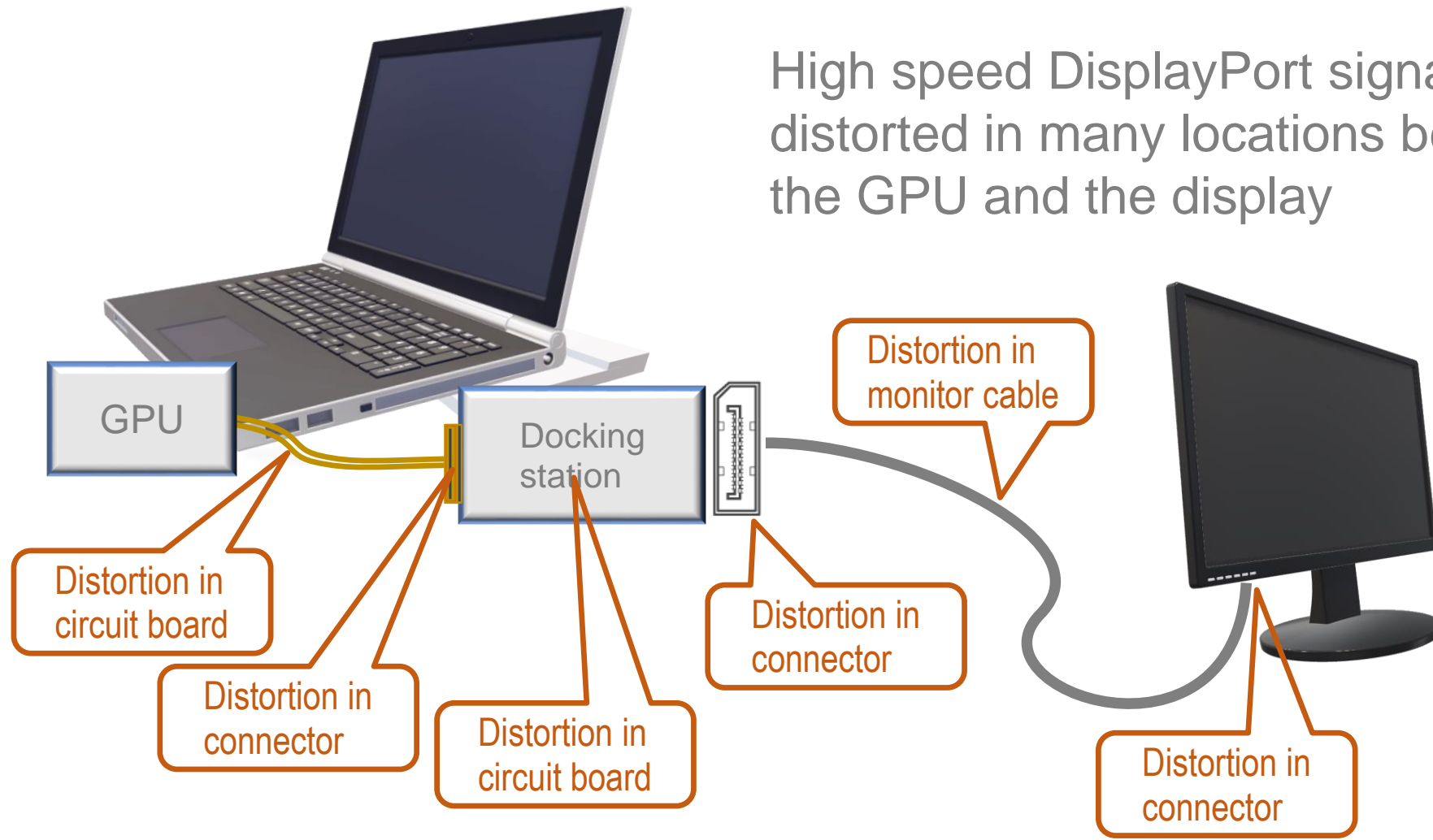
Link-Training Tunable PHY Repeaters

- What is a Link-Training Tunable PHY Repeater (LTTPR)?
- Why would you need a repeater?
- LTTPR features

- Example:
  - ✓ Recognizing LTTPRs
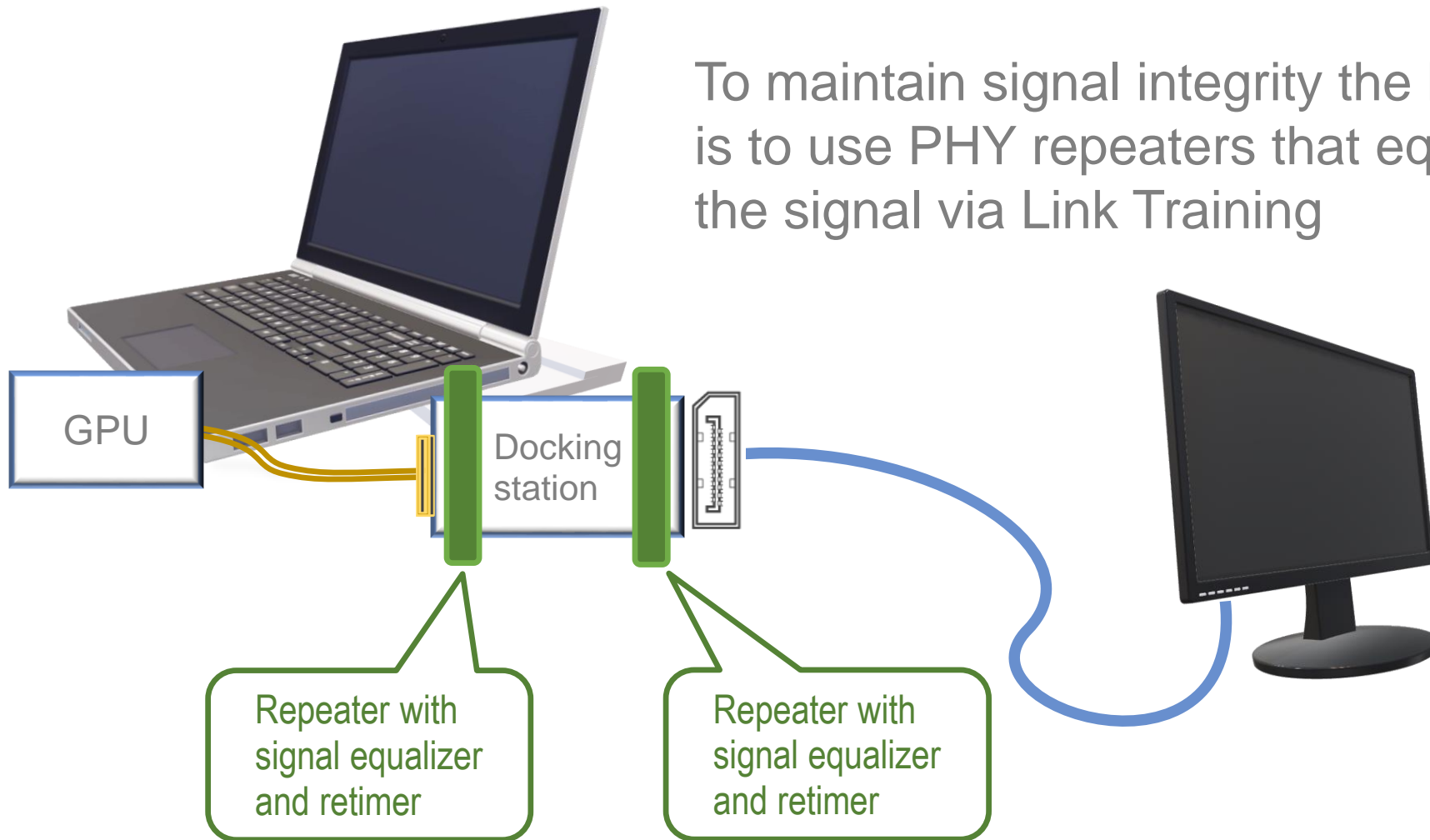 - ✓ Link training with LTTPRs.

PHY Repeaters

- A **PHY repeater** is a device containing only the PHY layer of data receiver and data transmitter for cleaning up signal waveform distortion caused by transmission across a cable, connector, or circuit board traces
- A PHY repeater does not contain encryption layer

- A PHY repeater that is capable of adjusting its output for Link Training is called Link-Training Tunable PHY Repeater

Why LTTPR?

UNIGRAF

High speed DisplayPort signal is distorted in many locations between the GPU and the display

GPU

Docking station

Distortion in monitor cable

Distortion in circuit board

Distortion in connector

Distortion in circuit board

Distortion in connector

Distortion in connector

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PHY Repeater Ensures Signal Integrity

- DisplayPort's high 8.1 Gbps/lane bit rate requires an active cable with PHY repeaters for cable lenghts exceeding 2 m .
- A USB Type-C cable longer than 1 m must have PHY repeaters to provide full performance.
  - ✓ Desktop computer connections typically require 2 m cables.
- Docking stations or "mini-docks" of laptop computers and USB Type-C connected equipment also need PHY repeaters

LTTPR Features

- LTTPR contains DP RX and DP TX PHY and a signal retimer
- LTTPR contains means for tuning the PHY parameters during LT
- LTTPR has up to four main Link Lanes and full Voltage Swing and Pre-emphasis combinations
- Specific DPCD register range (F0000h – F028Fh) for LTTPR use
- Up to 8 LTTPRs can be placed in the data path between DP Source, DP Sink or DP Repeater devices
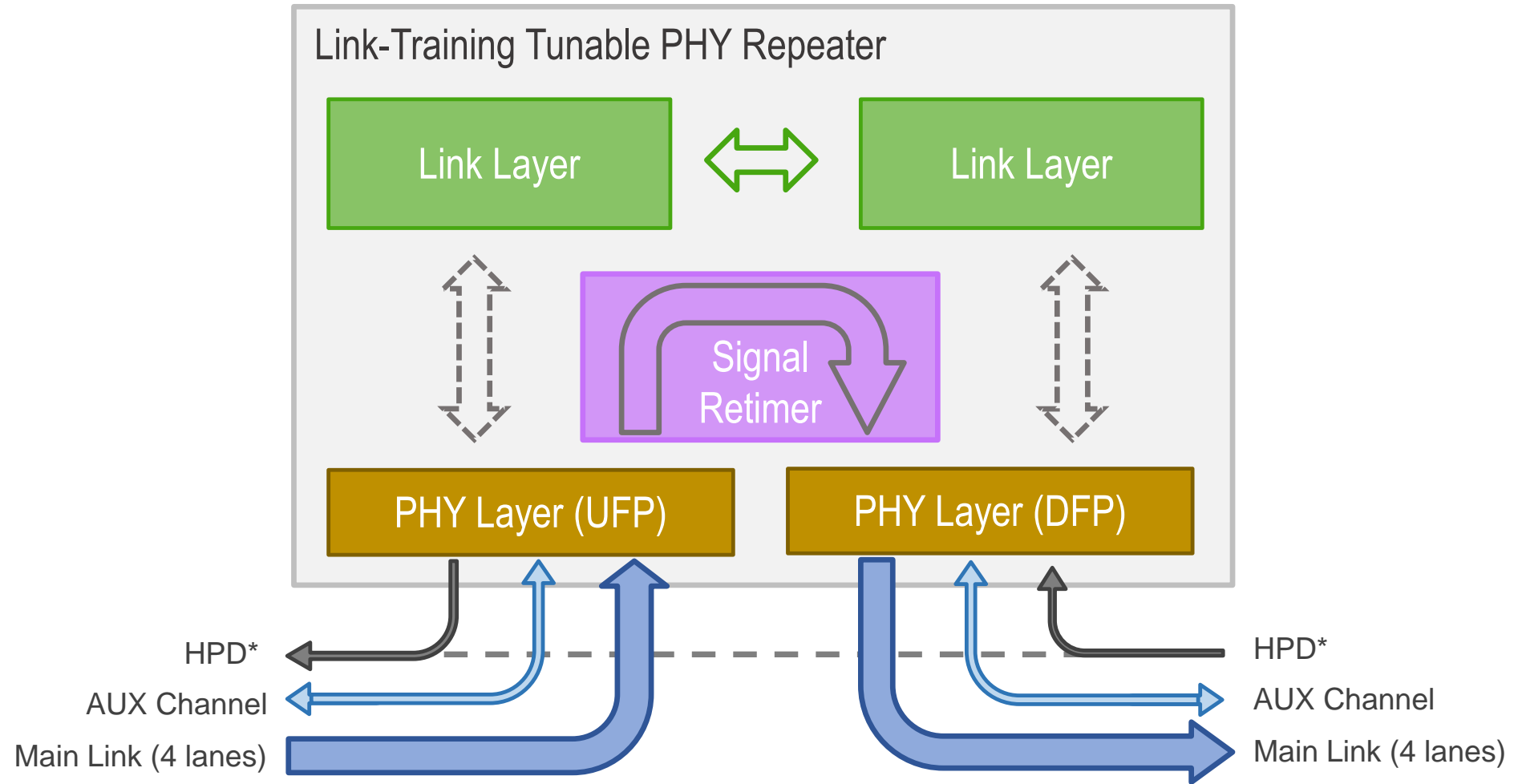
Two Operating Modes

Transparent Mode:
- Passes through all AUX transactions
- Snoops transactions to DPCD 00100h – 002FFh and updates output as needed

Non-transparent Mode:
- Replies to AUX transactions to LTTPR specific DPCD fields
- Passes through all other transactions
- Snoops transactions to DPCD 00100h – 002FFh and updates output as needed

DP Source controls LTTPR operating modes

LTTPR DPCD Registers

00000h – 000FFh
00100h – 002FFh
…
F0000h – F000Fh
F0010h – F005Fh
F0060h – F00AFh
…
F0240h – F028Fh
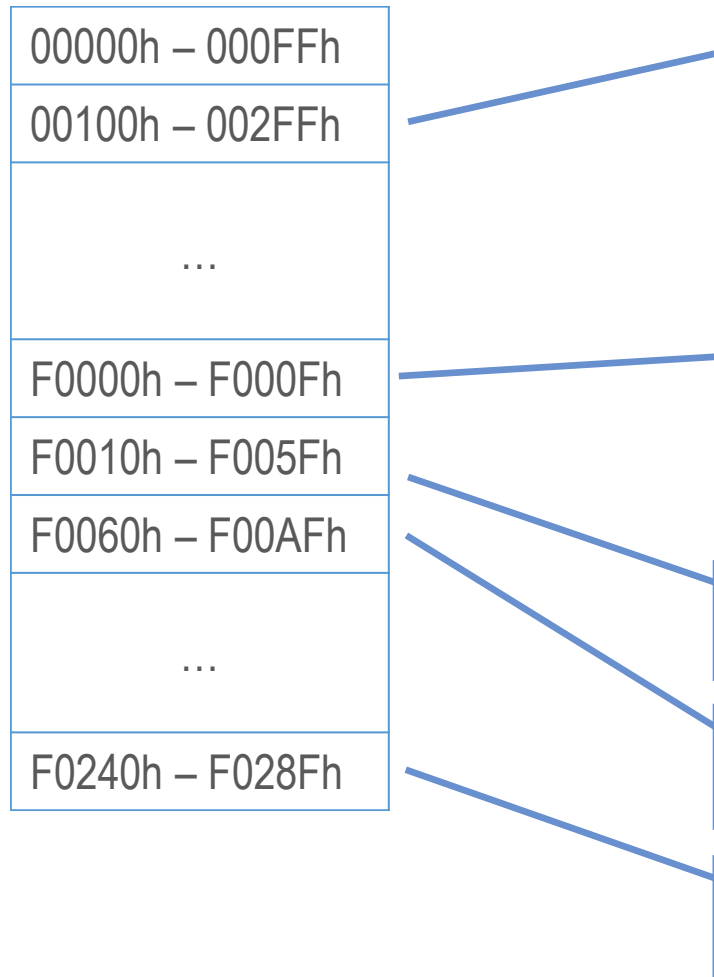
Link Configuration and Link/Sink Device Status
- *All LTTPRs shall snoop AUX transactions to these registers*
- *LTTPRs in Transparent Mode shall update output as needed*
- *LTTPR1 in Non-Transparent Mode shall update output as needed*

LT-tunable PHY Repeater DPCD Capability and ID Field
- *Shared by all LTTPRs between a DPTX and DPRX*
- *All LTTPRs shall replay to AUX transactions to these registers*

PHY_Repeater1 Configuration and Status
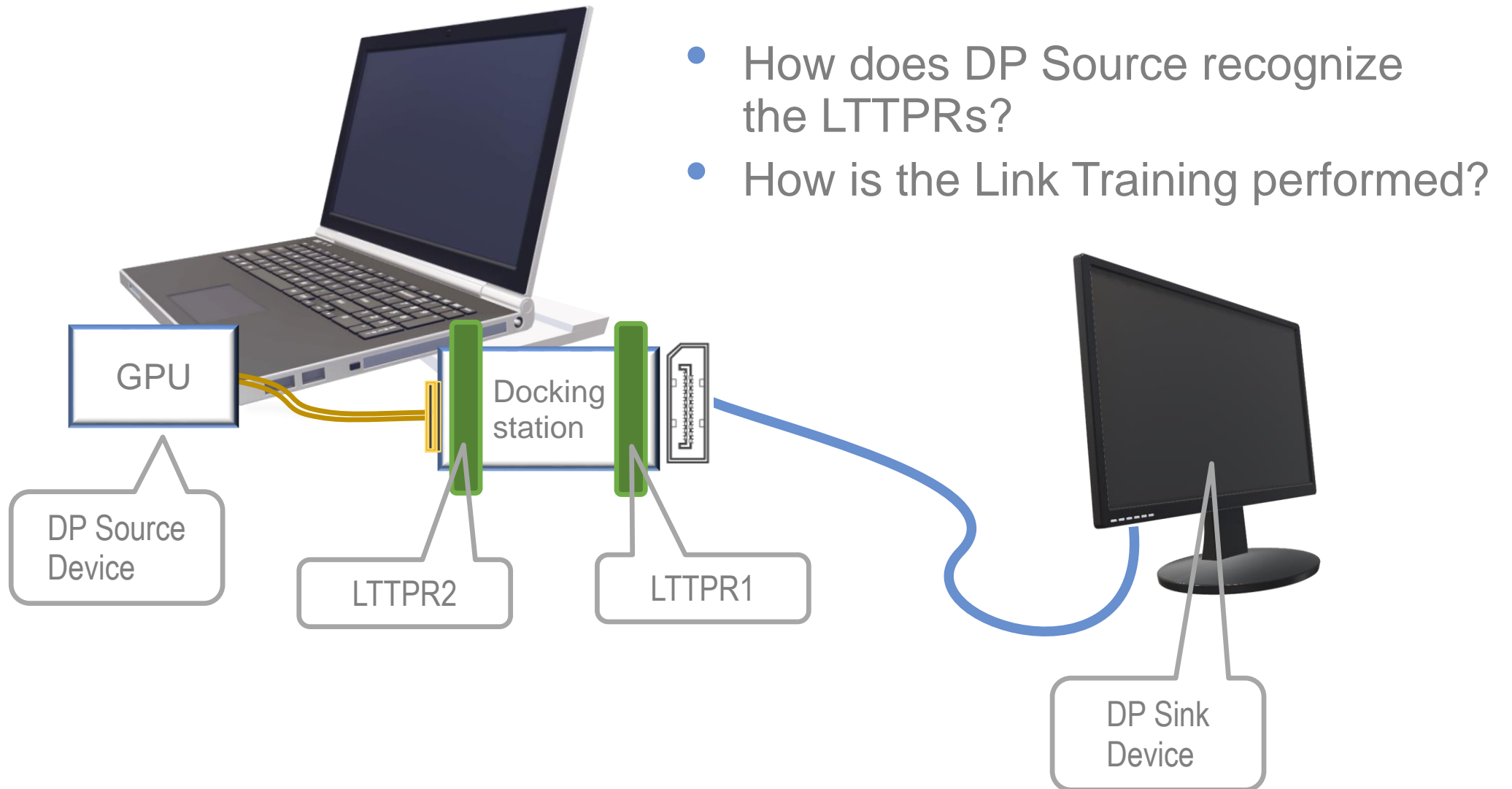- *Only LTTPR1 replies AUX transactions to these registers*

PHY_Repeater2 Configuration and Status
- *Only LTTPR2 replies AUX transactions to these registers*

PHY_Repeater8 Configuration and Status
- *Only LTTPR8 replies AUX transactions to these registers*

Example Configuration

- How does DP Source recognize the LTTPRs?
- How is the Link Training performed?

GPU

DP Source Device

Docking station
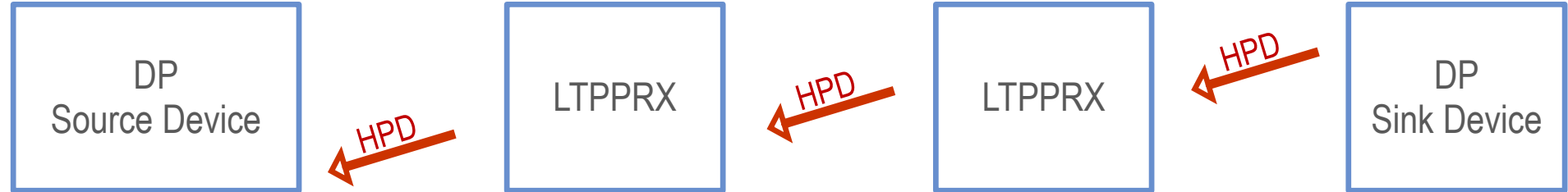
LTTPR2

LTTPR1

DP Sink Device
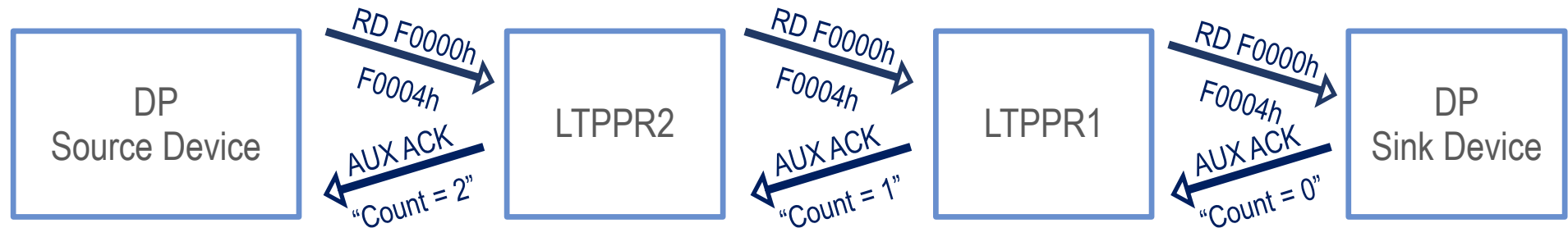
LTTPR Recognition

- Phase 1 (HPD is propagated):
  - ✓ HPD is asserted by DP Sink. All LTTPRs pass the signal.
- Phase 2 (Repeater count and capabilities):
  - ✓ DP Source reads DPCD F0000h to F0004h
  - ✓ DP Sink replies with zero data
  - ✓ LTTPR that receives zero count (LTTPR1) replaces it with its own data
  - ✓ Each LTTPR update the data with their capabilities and increment the count
- Phase 3 (DP Sink capabilities)
  - ✓ DP Source reads DPCD 00000h to 00002h
  - ✓ DP Sink replies with its capability data
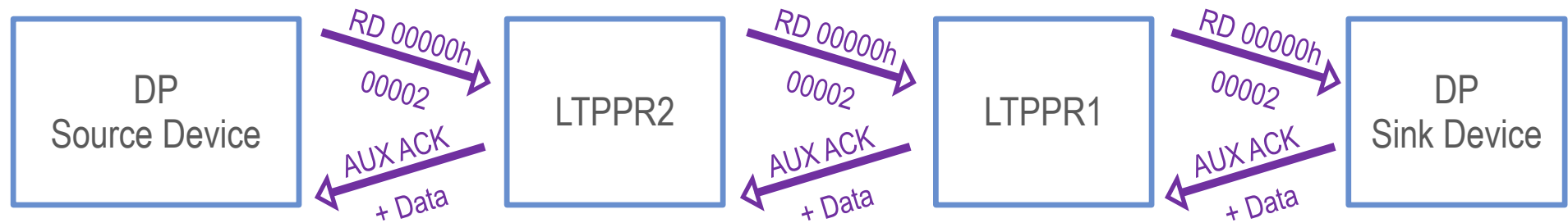 - ✓ Each LTTPR pass the information

LTTPR Recognition

1. Sink attached

DP Source Device ← HPD ← LTPPRX ← HPD ← LTPPRX ← HPD ← DP Sink Device

2. Detect LTTPRs

DP Source Device → RD F0000h F0004h → LTPPR2 → RD F0000h F0004h → LTPPR1 → RD F0000h F0004h → DP Sink Device

AUX ACK "Count = 2" ← / AUX ACK "Count = 1" ← / AUX ACK "Count = 0" ←

3. Read sink capabilities

DP Source Device → RD 00000h 00002 → LTPPR2 → RD 00000h 00002 → LTPPR1 → RD 00000h 00002 → DP Sink Device

AUX ACK + Data ← / AUX ACK + Data ← / AUX ACK + Data ←

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Link Training with LTTPRs

- DP Source performs full LT with each of the LTTPRs
  - ✓ LT starts with repeater closest to DP Source and ends with repeater closest to DP Sink
- DP Source writes to LTTPR specific LT registers
  - ✓ DP Sink and non-adressed LTTPRs reply AUX_NACK with $M = 0$
- DP Source reads LTTPR specific LT registers
  - ✓ DP Sink and non-adressed LTTPRs reply AUX_ACK with zero or copy data
- The LTTPR closest upstream snoops the data and sets its output accordingly
- When all LTTPRs have been trained, DP Source LT with DP Sink
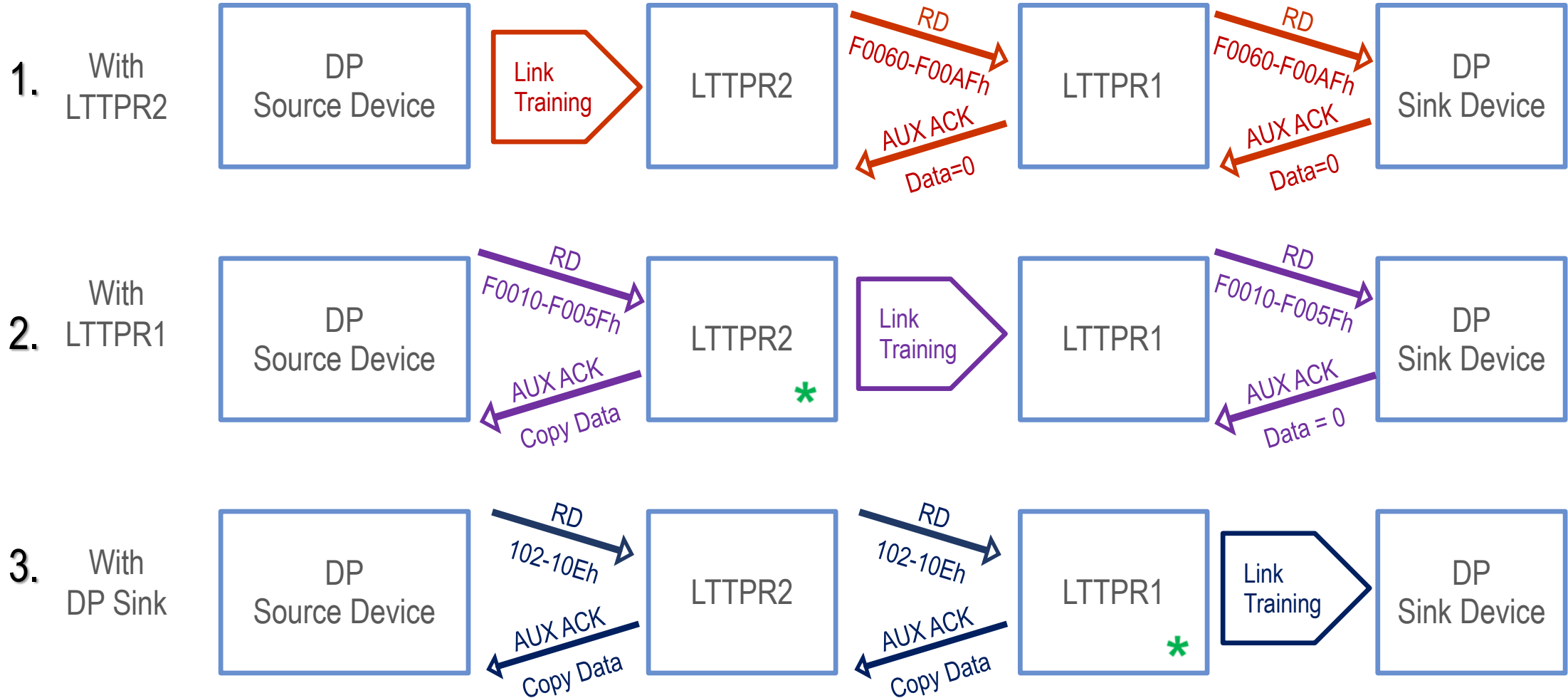
*) Snoop data and update output for LT

Unigraf UCD-400 Tester Supports LTTPR

- UCD-400 Features
  - ✓ Test DisplayPort 1.4 / HBR3 Sinks, Sources and Repeaters
  - ✓ Capture and Source up to 8K@30 & 4K@120 video and audio
  - ✓ Verify HDCP 1.3 and HDCP 2.2 operation;
    Run HDCP 2.2 Compliance Test
  - ✓ Monitor link status, set configuration parameters
  - ✓ USB 3.0 connected
- *UCD Console* GUI for debugging
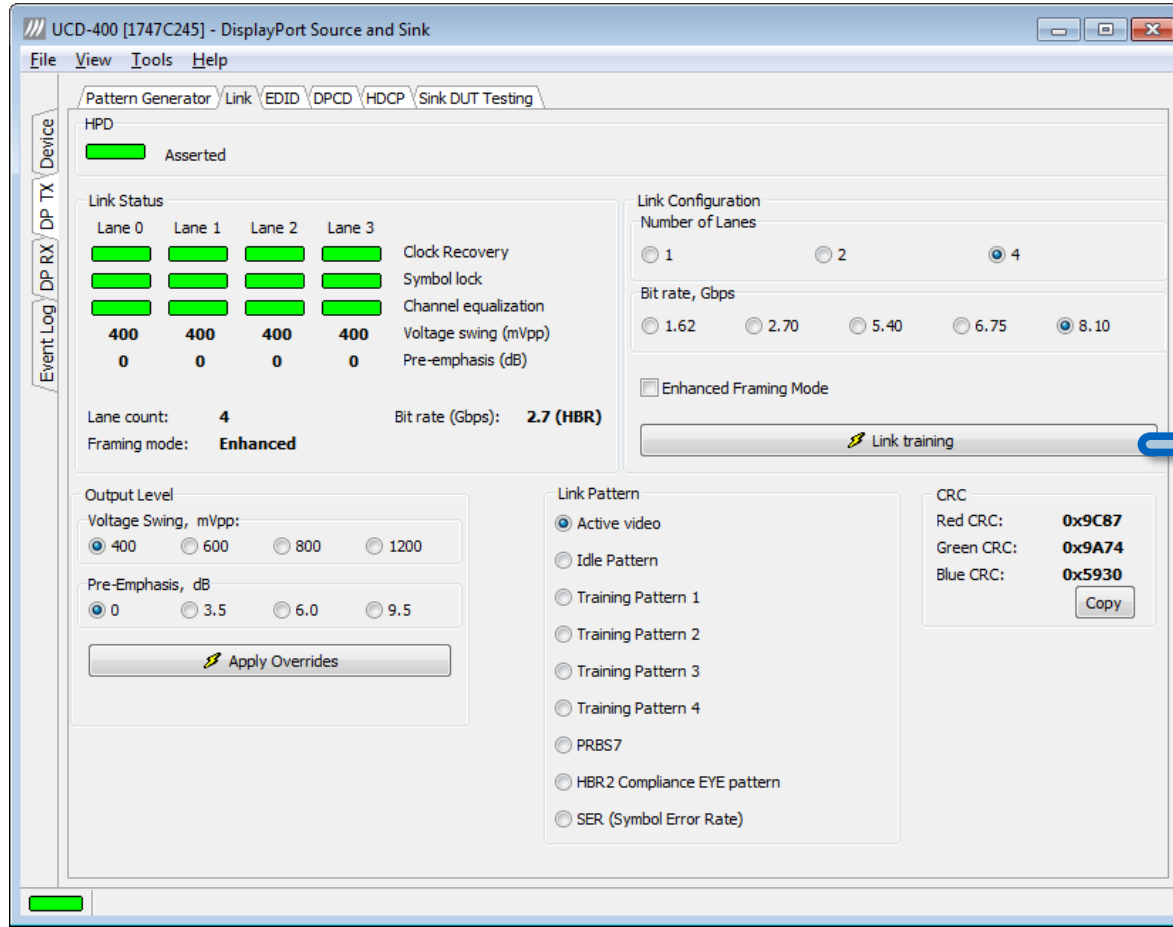- High level *TSI API* for easy integration

UCD Console GUI

Reference Sink
(Test Source DUT)

Reference Source
(Test Sink DUT)

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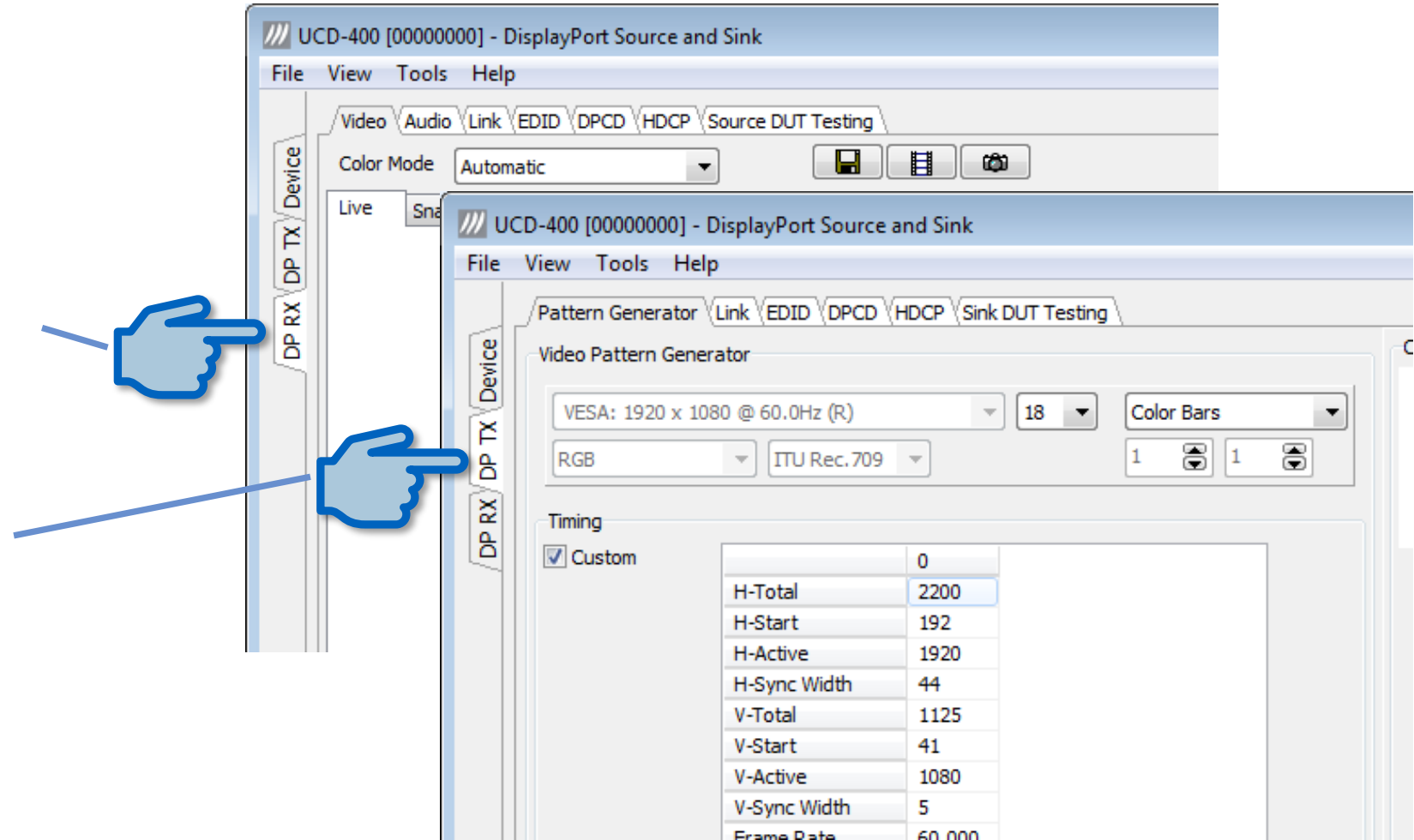
LT with UCD Console

In order to perform Link Training with LTTPRs click here

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Thank You!

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