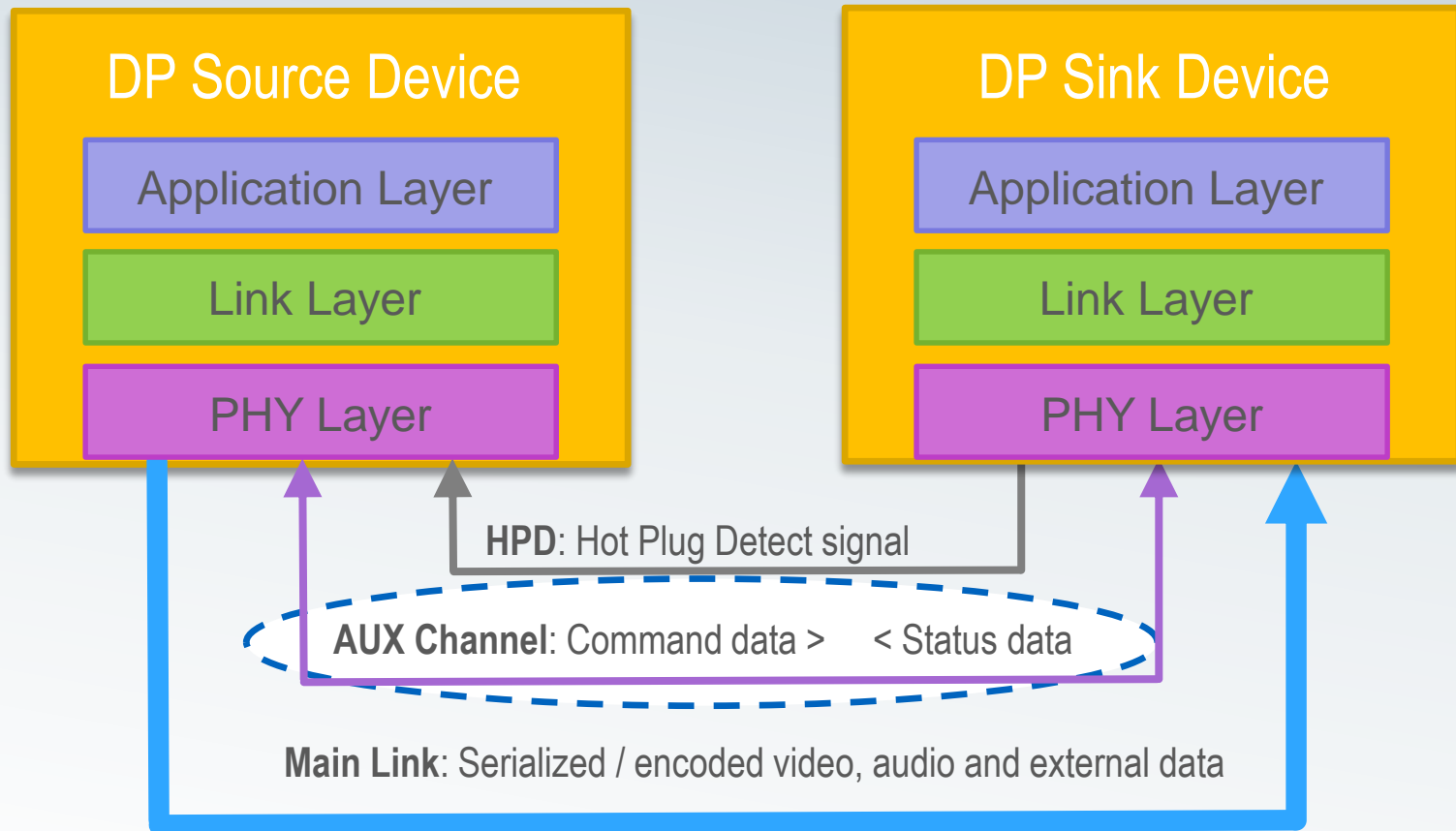




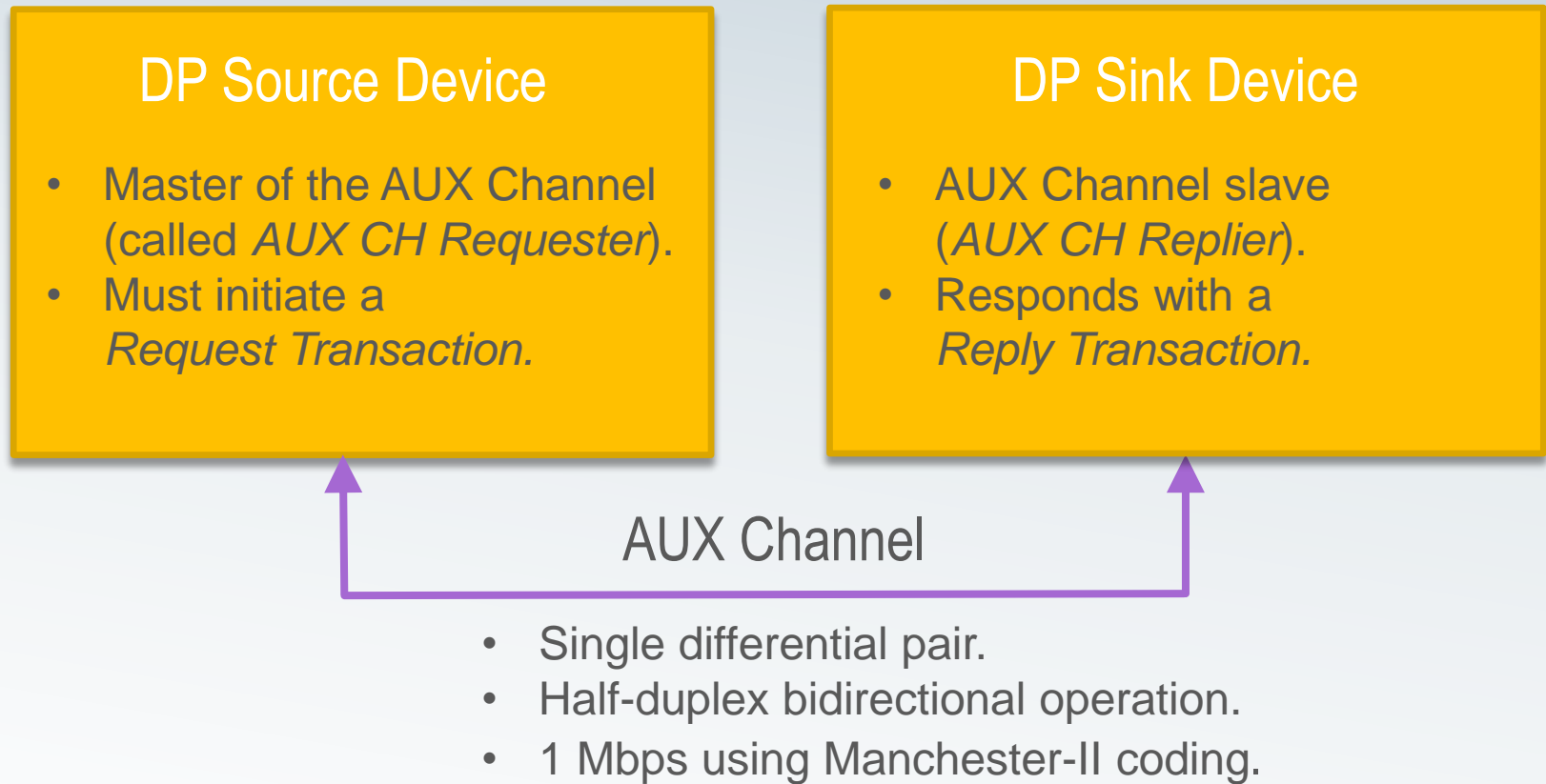
# How to Monitor AUX Channel Communication of DisplayPort Interfaces



# DisplayPort Interface



# AUX Channel Topology



# Use of AUX Channel

## AUX Link Services

- Link Capability Read
- Link Configuration (training)
- Link Status Read

## AUX Device Services

- EDID Read
- MCCS (Monitor Command and Control Set) support
- Sink Event Notification

## Sideband Messaging

- Send & Receive Messages from Remote DP Nodes
- Report MST Status Changes and Errors

# AUX Channel Protocol Example 1

## Read from Sink DPCD

| Source                     |             | Sink             |       |
|----------------------------|-------------|------------------|-------|
| Req RD 1 byte from 0x00218 | 90 02 19 00 | AUX ACK (1 byte) | 00 00 |

Source: Read one byte of data from DPCD 0x00218

Sink: OK,

TEST\_REQUEST (Test requested by the Sink device):

0x00218 := 0x00

TEST\_LINK\_TRAINING = 0

TEST\_VIDEO\_PATTERN = 0

TEST\_EDID\_READ = 0

PHY\_TEST\_PATTERN = 0

FAUX\_TEST\_PATTERN = 0

*Please refer to: DP v1.2a: 2.9.3.1 Address Mapping for Link Configuration/Management*

# AUX Channel Protocol Example 2

## Write to Sink DPCD

| Source                    |                            | Sink |    |
|---------------------------|----------------------------|------|----|
| Req WR 5 bytes to 0x00102 | 80 01 02 04 22 38 38 38 38 | ACK  | 00 |

Source: Write 5 bytes of data to DPCD 0x00102

TRAINING\_PATTERN\_SET (0x00102 := 0x22)

TRAINING\_PATTERN\_SET = 2 (Pattern 2)

RECOVERED\_CLOCK\_OUT\_EN = 0

SCRAMBLING\_DISABLE = 1

SYMBOL\_ERROR\_COUNT\_SEL = 0 (Disparity and Illegal Symbol)

TRAINING\_LANE0\_SET (Link Training Control, Lane 0)(0x00103 := 0x38)

VOLTAGE\_SWING\_SET = level 0

MAX\_SWING\_REACHED = 0

PRE\_EMPHASIS\_SET = level 3

MAX\_PRE-EMPHASIS\_REACHED = 1 etc. ...

Sink: OK

*Please refer to: DP v1.2a 2.9.3.1 Address Mapping for Link Configuration/Management*

# AUX Channel Protocol Example 3

## Sideband Message - step 1 (Request)

| Source                    |                            | Sink |    |
|---------------------------|----------------------------|------|----|
| Req WR 5 bytes to 0x01000 | 80 10 00 04 10 02 cb 01 d5 | ACK  | 00 |

DOWN\_REQ - REQ: LINK\_ADDRESS

-- Sideband message header --

Link\_Count\_Total = 1

Link\_Count\_Remaining = 0

Broadcast\_Message = 0

Path\_Message = 0

MSG\_Body\_Length = 2

Start\_Of\_MT = 1

End\_Of\_MT = 1

Message\_Sequence\_No = 0

*Please refer to: DP v1.2a 2.9.3.1 Address Mapping for Link Configuration/Management*

# AUX Channel Protocol Example 3

## Sideband Message - step 2 (Enquire Reply)

| Source                      |             | Sink              |       |
|-----------------------------|-------------|-------------------|-------|
| Req RD 1 bytes from 0x02003 | 90 20 03 00 | AUX_ACK - 1 bytes | 00 10 |

DEVICE\_SERVICE\_IRQ\_VECTOR\_ESI0 [CLR] [1.2]

0x02003 := 0x10

(Reserved) REMOTE\_CONTOL\_COMMAND\_PENDING = 0

AUTOMATED\_TEST\_REQUEST = 0

CP\_IRQ = 0

MCCS\_IRQ = 0

**DOWN\_REP\_MSG\_RDY = 1**

UP\_REQ\_MSG\_RDY = 0

SINK\_SPECIFIC\_IRQ = 0

*Please refer to: DP v1.2a 2.9.3.1 Address Mapping for Link Configuration/Management*



# AUX Channel Protocol Example 3

## Sideband Message - step 3 (Reply)

| Source                          |             | Sink               |   |
|---------------------------------|-------------|--------------------|---|
| Req RD 16 bytes from<br>0x01410 | 90 14 10 0f | AUX_ACK - 16 bytes | 00 22 93 1a 45 03 90 c0 4b<br>00 00 00 00 00 00 00 00 |

DOWN\_REP - Message Transaction fragment

-- Sideband message header --

Link\_Count\_Total = 1

Link\_Count\_Remaining = 0

Broadcast\_Message = 0

Path\_Message = 0

MSG\_Body\_Length = 21

Start\_Of\_MT = 1

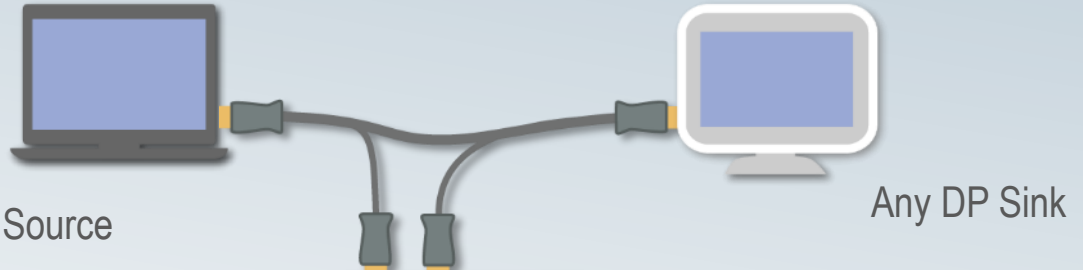
End\_Of\_MT = 0

Message\_Sequence\_No = 0

Etc. ...

*Please refer to: DP v1.2a 2.9.3.1 Address Mapping for Link Configuration/Management*

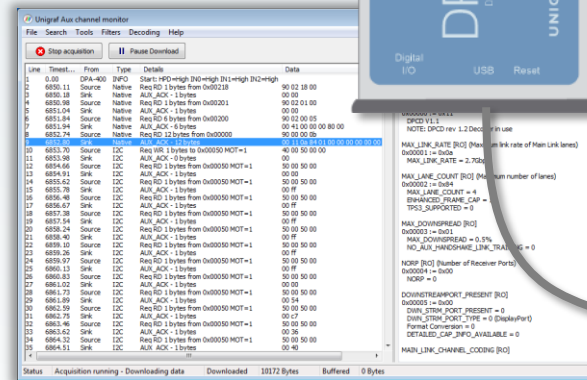
# AUX Monitor



## Equipment:

- DPA-400 1.2 unit
- Unigraf "Y" cable
- AUX Channel Monitor GUI

AUX  
Monitor  
GUI



USB

Host PC

# DPR-120 Embedded AUX Monitor



DP Source

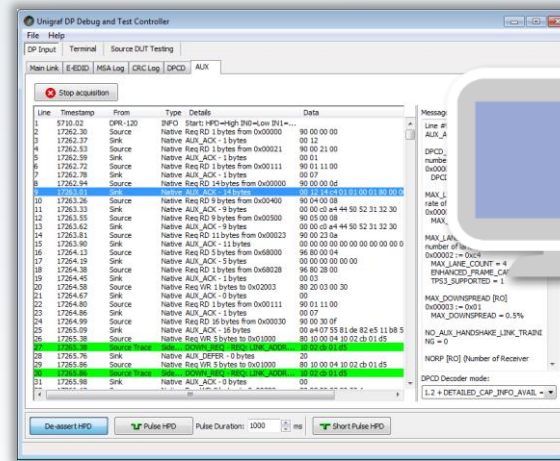
DP Reference Sink



## Equipment:

- DPR-120 unit
- Debug and Test Controller GUI
- *MST Debug Extension* option

Debug and Test  
Controller GUI  
Embedded  
AUX Monitor  
Tab



USB

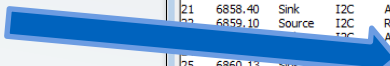
Host PC

# Unigraf AUX Monitor GUI

Log controls



AUX Channel transaction log



The screenshot shows the Unigraf Aux channel monitor interface. At the top, there are menu options: File, Search, Tools, Filters, Decoding, Help. Below the menu are two buttons: 'Stop acquisition' (with a red 'X' icon) and 'Pause Download' (with a pause icon). The main area is divided into two panes. The left pane is a table with columns: Line, Timest..., From, Type, Details, and Data. The right pane is titled 'Message details:' and shows a list of parameters and their values for a specific transaction.

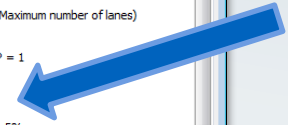
| Line | Timest... | From    | Type   | Details                                    | Data                             |
|------|-----------|---------|--------|--|----------------------------------|
| 1    | 0.00      | DPA-400 | INFO   | Start: HPD=High IN0=High IN1=High IN2=High |                                  |
| 2    | 6850.11   | Source  | Native | Req RD 1 bytes from 0x00218                | 90 02 18 00                      |
| 3    | 6850.18   | Sink    | Native | AUX_ACK - 1 bytes                          | 00 00                            |
| 4    | 6850.98   | Source  | Native | Req RD 1 bytes from 0x00201                | 90 02 01 00                      |
| 5    | 6851.04   | Sink    | Native | AUX_ACK - 1 bytes                          | 00 00                            |
| 6    | 6851.84   | Source  | Native | Req RD 6 bytes from 0x00200                | 90 02 00 05                      |
| 7    | 6851.94   | Sink    | Native | AUX_ACK - 6 bytes                          | 00 41 00 00 00 80 00             |
| 8    | 6852.74   | Source  | Native | Req RD 12 bytes from 0x00000               | 90 00 00 0b                      |
| 9    | 6852.80   | Sink    | Native | AUX_ACK - 12 bytes                         | 00 11 0a 84 01 00 00 00 00 00 00 |
| 10   | 6853.70   | Source  | I2C    | Req WR 1 bytes to 0x00050 MOT=1            | 40 00 50 00 00                   |
| 11   | 6853.98   | Sink    | I2C    | AUX_ACK - 0 bytes                          | 00                               |
| 12   | 6854.66   | Source  | I2C    | Req RD 1 bytes from 0x00050 MOT=1          | 50 00 50 00                      |
| 13   | 6854.91   | Sink    | I2C    | AUX_ACK - 1 bytes                          | 00 00                            |
| 14   | 6855.62   | Source  | I2C    | Req RD 1 bytes from 0x00050 MOT=1          | 50 00 50 00                      |
| 15   | 6855.78   | Sink    | I2C    | AUX_ACK - 1 bytes                          | 00 ff                            |
| 16   | 6856.48   | Source  | I2C    | Req RD 1 bytes from 0x00050 MOT=1          | 50 00 50 00                      |
| 17   | 6856.67   | Sink    | I2C    | AUX_ACK - 1 bytes                          | 00 ff                            |
| 18   | 6857.38   | Source  | I2C    | Req RD 1 bytes from 0x00050 MOT=1          | 50 00 50 00                      |
| 19   | 6857.54   | Sink    | I2C    | AUX_ACK - 1 bytes                          | 00 ff                            |
| 20   | 6858.24   | Source  | I2C    | Req RD 1 bytes from 0x00050 MOT=1          | 50 00 50 00                      |
| 21   | 6858.40   | Sink    | I2C    | AUX_ACK - 1 bytes                          | 00 ff                            |
| 22   | 6859.10   | Source  | I2C    | Req RD 1 bytes from 0x00050 MOT=1          | 50 00 50 00                      |
| 23   | 6859.26   | Sink    | I2C    | AUX_ACK - 1 bytes                          | 00 ff                            |
| 24   | 6860.00   | Source  | I2C    | Req RD 1 bytes from 0x00050 MOT=1          | 50 00 50 00                      |
| 25   | 6860.13   | Sink    | I2C    | AUX_ACK - 1 bytes                          | 00 ff                            |
| 26   | 6860.83   | Source  | I2C    | Req RD 1 bytes from 0x00050 MOT=1          | 50 00 50 00                      |
| 27   | 6861.02   | Sink    | I2C    | AUX_ACK - 1 bytes                          | 00 00                            |
| 28   | 6861.73   | Source  | I2C    | Req RD 1 bytes from 0x00050 MOT=1          | 50 00 50 00                      |
| 29   | 6861.89   | Sink    | I2C    | AUX_ACK - 1 bytes                          | 00 54                            |
| 30   | 6862.59   | Source  | I2C    | Req RD 1 bytes from 0x00050 MOT=1          | 50 00 50 00                      |
| 31   | 6862.75   | Sink    | I2C    | AUX_ACK - 1 bytes                          | 00 c7                            |
| 32   | 6863.46   | Source  | I2C    | Req RD 1 bytes from 0x00050 MOT=1          | 50 00 50 00                      |
| 33   | 6863.62   | Sink    | I2C    | AUX_ACK - 1 bytes                          | 00 36                            |
| 34   | 6864.32   | Source  | I2C    | Req RD 1 bytes from 0x00050 MOT=1          | 50 00 50 00                      |
| 35   | 6864.51   | Sink    | I2C    | AUX_ACK - 1 bytes                          | 00 40                            |

The 'Message details' pane shows the following information for Line #9 (6852.80ms):

- AUX\_ACK - 12 bytes
- DPCD\_REV [RO] (DPCD revision number): 0x00000 := 0x11
- DPCD v1.1
- NOTE: DPCD rev 1.2 Decoder in use
- MAX\_LINK\_RATE [RO] (Maximum link rate of Main Link lanes): 0x00001 := 0x0a
- MAX\_LINK\_RATE = 2.7Gbps
- MAX\_LANE\_COUNT [RO] (Maximum number of lanes): 0x00002 := 0x84
- MAX\_LANE\_COUNT = 4
- ENHANCED\_FRAME\_CAP = 1
- TPSS\_SUPPORTED = 0
- MAX\_DOWNSPREAD [RO]: 0x00003 := 0x01
- MAX\_DOWNSPREAD = 0.5%
- NO\_AUX\_HANDSHAKE\_LINK\_TRAINING = 0
- NORP [RO] (Number of Receiver Ports): 0x00004 := 0x00
- NORP = 0
- DOWNSTREAMPORT\_PRESENT [RO]: 0x00005 := 0x00
- DWN\_STRM\_PORT\_PRESENT = 0
- DWN\_STRM\_PORT\_TYPE = 0 (DisplayPort)
- Format Conversion = 0
- DETAILED\_CAP\_INFO\_AVAILABLE = 0
- MAIN\_LINK\_CHANNEL\_CODING [RO]

At the bottom of the window, the status bar shows: Status Acquisition running - Downloading data Downloaded 10172 Bytes Buffered 0 Bytes

Parsed interpretation of one transaction



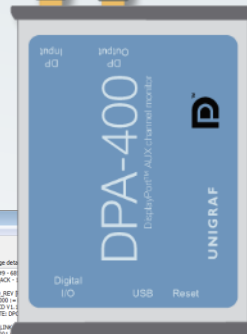
# Case: Interoperability Testing



DP Source



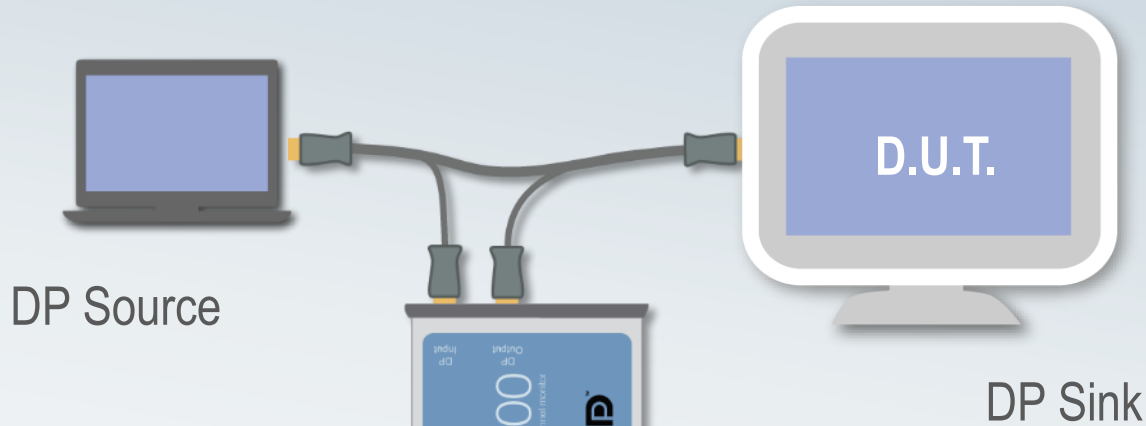
DP Sink



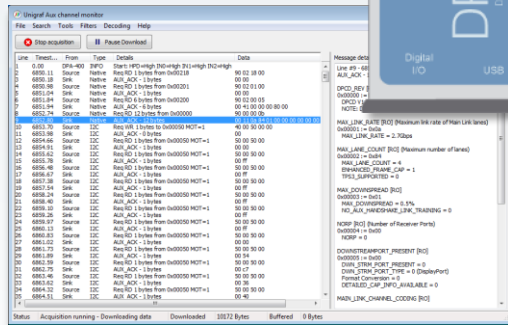
AUX Monitor GUI

| Line  | Time     | From    | Type                             | Details                                | Data                                |
|-------|----------|---------|----------------------------------|--|-------------------------------------|
| 0.00  | 00:00:00 | DPA-400 | DPD                              | Start #F0-high D0-high D1-high D2-high |                                     |
| 0.000 | 00:00:00 | Source  | ReqID 1 bytes from D0001E8       |  | 00 00 00 00                         |
| 0.000 | 00:00:00 | Sink    | ReqID 1 bytes from D000201       |  | 00 00 00 00                         |
| 0.001 | 00:00:00 | Source  | ReqID 1 bytes from D000200       |  | 00 00 00 00                         |
| 0.001 | 00:00:00 | Sink    | ReqID 1 bytes from D000200       |  | 00 00 00 00                         |
| 0.002 | 00:00:00 | Source  | ReqID 12 bytes from D000000      |  | 00 00 00 00 00 00 00 00 00 00 00 00 |
| 0.002 | 00:00:00 | Sink    | ReqID 12 bytes from D000000      |  | 00 00 00 00 00 00 00 00 00 00 00 00 |
| 0.003 | 00:00:00 | Source  | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.003 | 00:00:00 | Sink    | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.004 | 00:00:00 | Source  | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.004 | 00:00:00 | Sink    | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.005 | 00:00:00 | Source  | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.005 | 00:00:00 | Sink    | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.006 | 00:00:00 | Source  | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.006 | 00:00:00 | Sink    | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.007 | 00:00:00 | Source  | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.007 | 00:00:00 | Sink    | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.008 | 00:00:00 | Source  | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.008 | 00:00:00 | Sink    | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.009 | 00:00:00 | Source  | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.009 | 00:00:00 | Sink    | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.010 | 00:00:00 | Source  | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.010 | 00:00:00 | Sink    | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.011 | 00:00:00 | Source  | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.011 | 00:00:00 | Sink    | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.012 | 00:00:00 | Source  | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.012 | 00:00:00 | Sink    | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.013 | 00:00:00 | Source  | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.013 | 00:00:00 | Sink    | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.014 | 00:00:00 | Source  | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.014 | 00:00:00 | Sink    | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.015 | 00:00:00 | Source  | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.015 | 00:00:00 | Sink    | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.016 | 00:00:00 | Source  | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.016 | 00:00:00 | Sink    | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.017 | 00:00:00 | Source  | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.017 | 00:00:00 | Sink    | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.018 | 00:00:00 | Source  | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.018 | 00:00:00 | Sink    | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.019 | 00:00:00 | Source  | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.019 | 00:00:00 | Sink    | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.020 | 00:00:00 | Source  | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.020 | 00:00:00 | Sink    | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.021 | 00:00:00 | Source  | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.021 | 00:00:00 | Sink    | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.022 | 00:00:00 | Source  | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.022 | 00:00:00 | Sink    | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.023 | 00:00:00 | Source  | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.023 | 00:00:00 | Sink    | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.024 | 00:00:00 | Source  | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.024 | 00:00:00 | Sink    | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.025 | 00:00:00 | Source  | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |
| 0.025 | 00:00:00 | Sink    | ReqID 1 bytes from D000000 MCT+1 |  | 00 00 00 00                         |

# Case: Interoperability Testing



AUX  
Monitor  
GUI

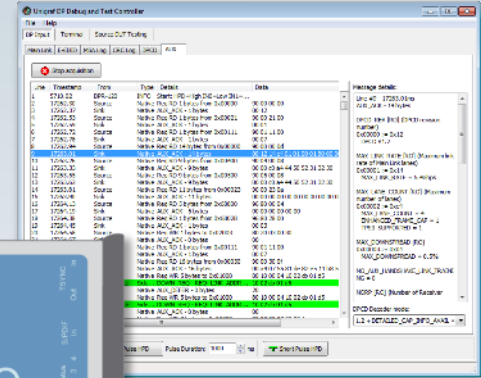


# Case: Link Compliance Testing

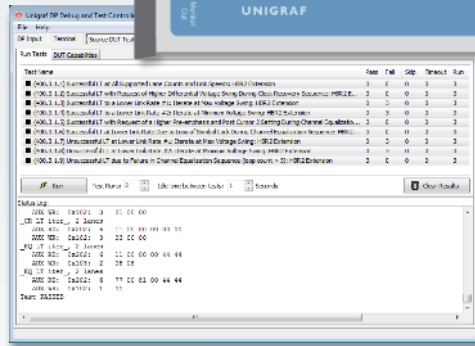


DP Source

DP Reference Sink



Embedded AUX Monitor Tab

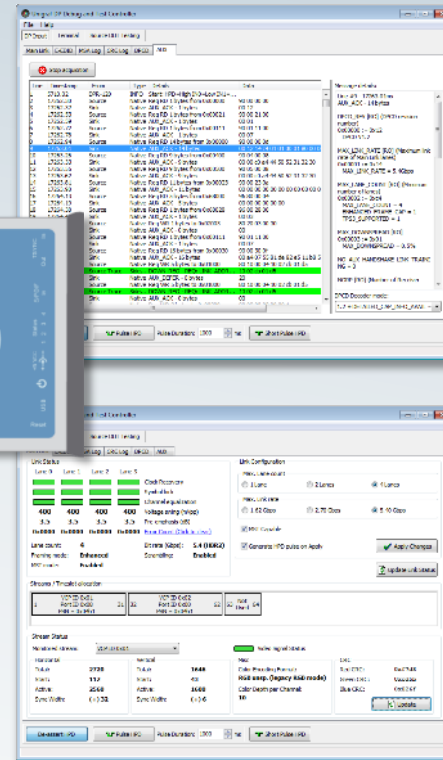
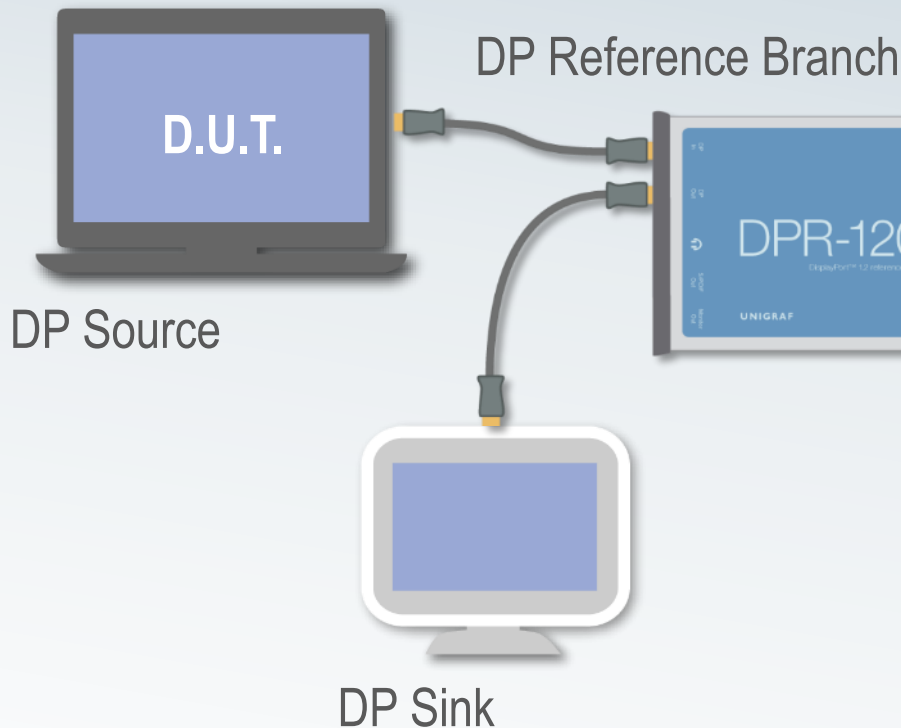


Compliance Testing Tab

Both tools in DPR-120 Debug and Test Controller GUI



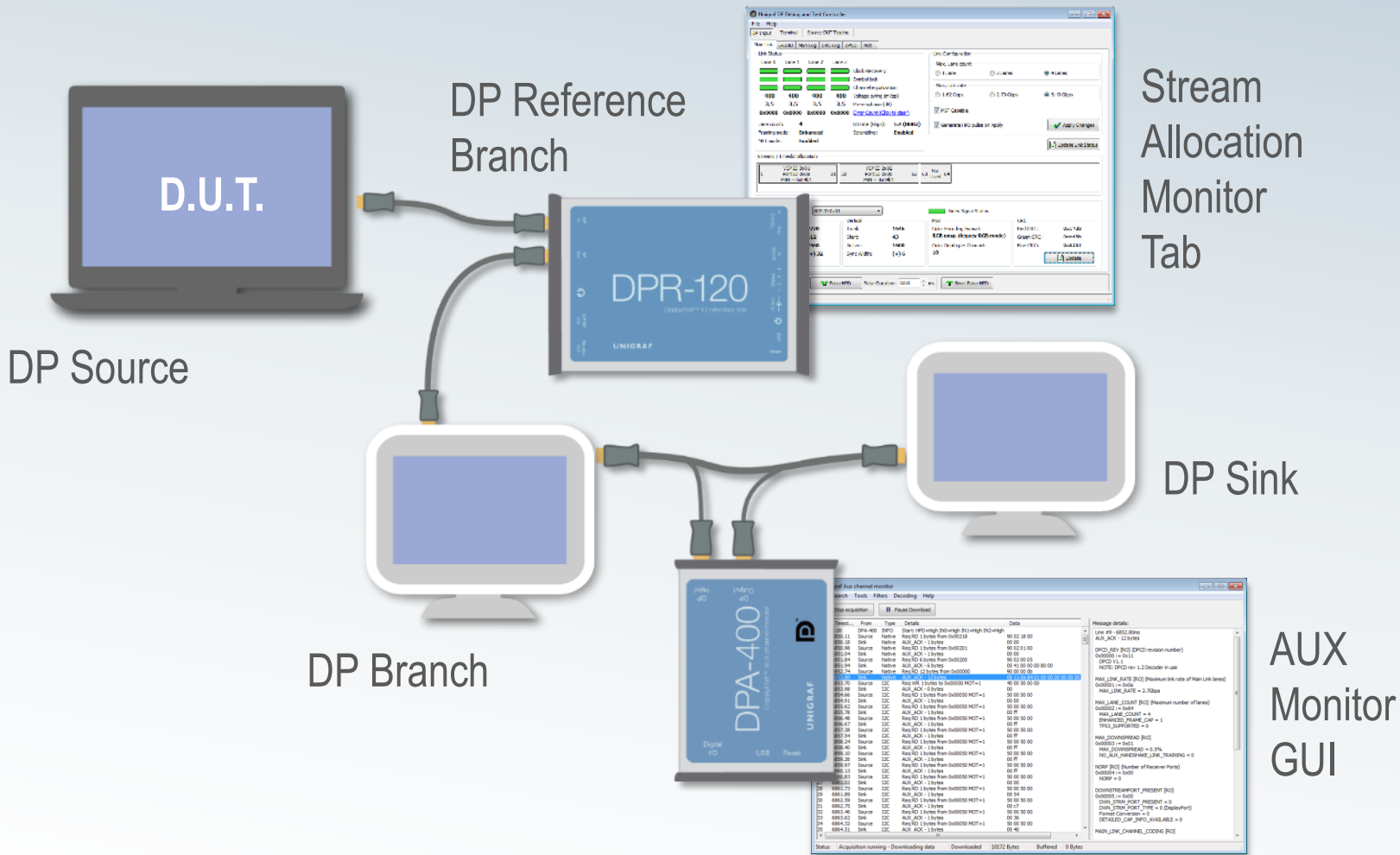
# Case: MST Interoperability Testing



Both tools in DPR-120  
Debug and Test Controller GUI



# Case: MST Interoperability Testing



# Case: MST Interoperability Testing

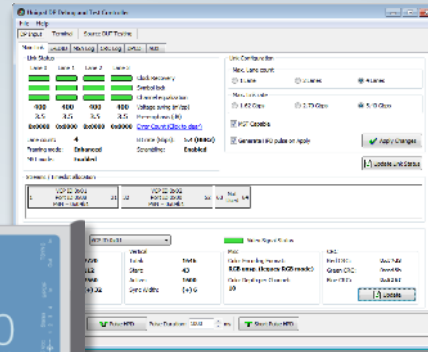
DP Source



DP Reference Branch



Stream Allocation Monitor Tab



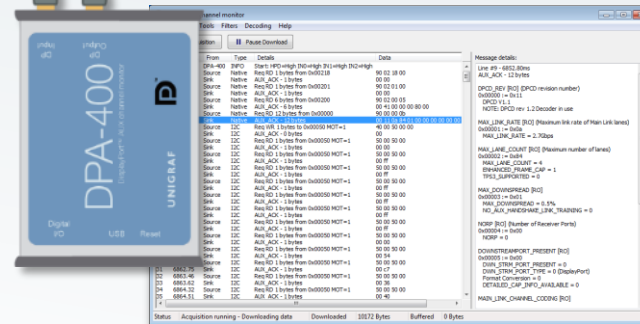
DP Sink



D.U.T.

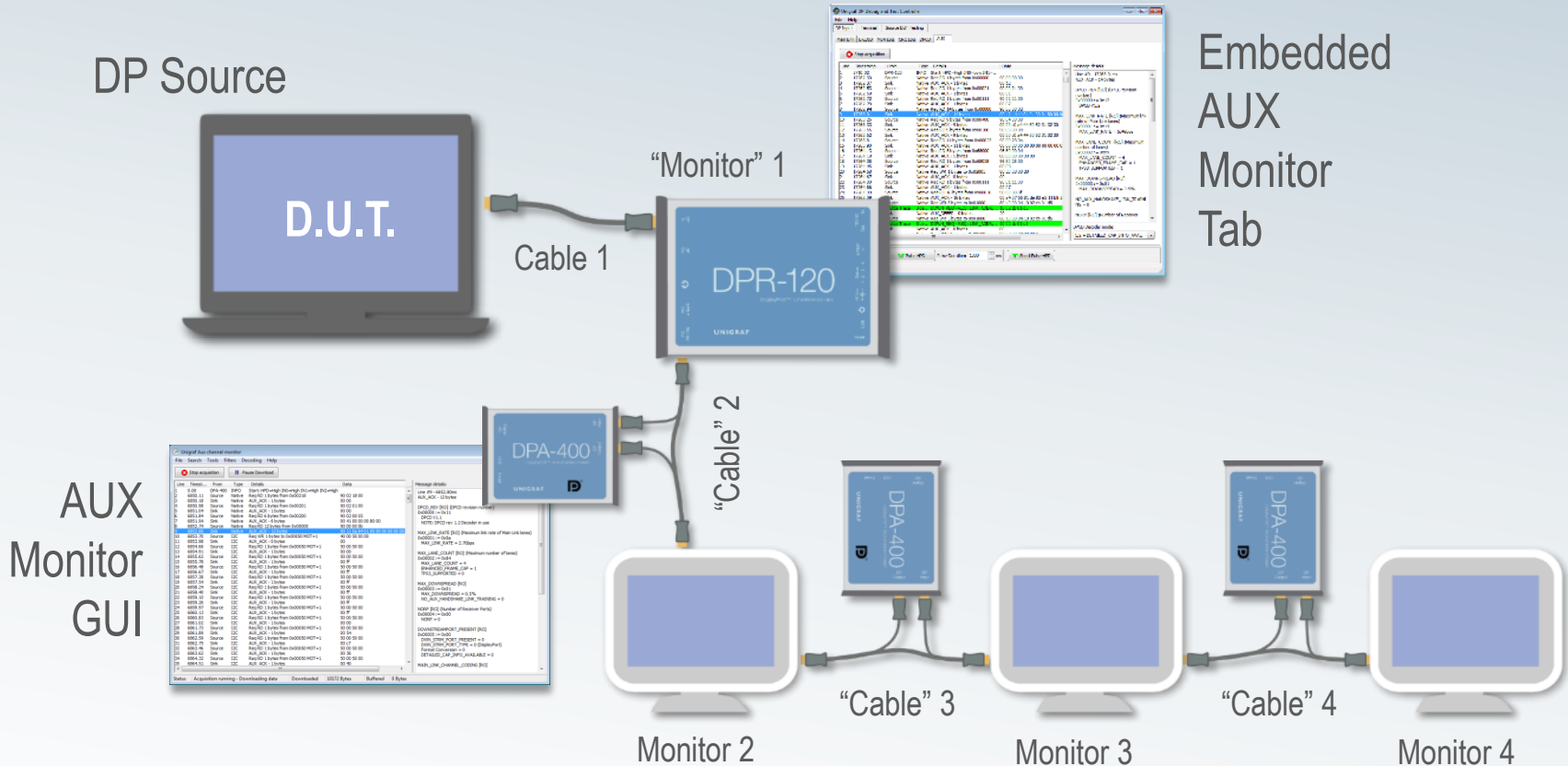


DP Branch



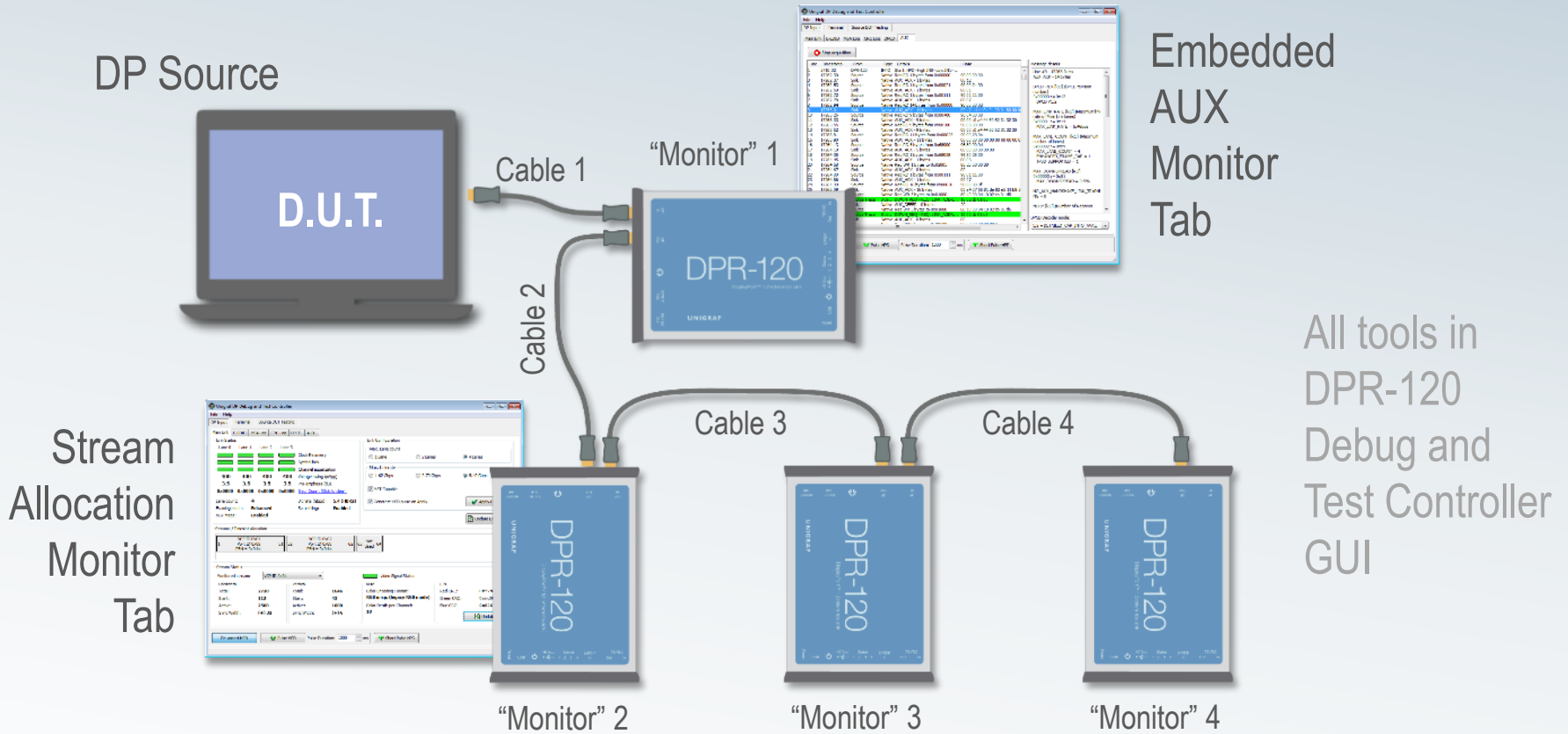
AUX Monitor GUI

# DisplayPort MST Interoperability Test Procedure



Please refer to: *VESA DisplayPort® Multi-Stream Transport Certification Test Procedure; Revision D*

# DisplayPort MST Interoperability Test Procedure



Please refer to: *VESA DisplayPort® Multi-Stream Transport Certification Test Procedure; Revision D*

# Summary

- DPA-400 Advantages:
  - ✓ Can be used between any Source and Sink
  - ✓ Needed between MST Branch and Sink
- DPR-120 Built-in AUX Advantages:
  - ✓ Link CTS tool and AUX Monitor in the same GUI
  - ✓ Reduces the # of connectors in the stream path



# Thank You!

Please visit [www.unigraf.fi](http://www.unigraf.fi)  
for more information.